Muon Port Card FPGA Mezzanine, Revision 2, May 2011

- XCF32P PROM
- XCF128X PROM
- PQ035ZN1HZPH Voltage Regulator for the FPGA core (1.0V @ 1.5A)
- LP38853S Voltage Regulator for the FPGA core (1.0V @ 3A)

CLOCK DRIVERS
New Features for Revision 2, May 2011

- **Two PROM Options:**
  - XCF32P
    - 4MByte
    - 8-bit parallel interface to FPGA
    - direct access via JTAG
  - XCF128X
    - 16MByte
    - 16-bit parallel interface to FPGA
    - indirect access through the FPGA

- **Two Voltage Regulators for the FPGA Core Voltage 1.0V:**
  - PQ035ZN1HZPH (1.5A)
  - LP38853S (3.0A)

- **80MHz/120MHz Clock Drivers for 12 TLK2501 Serializers**
Status as of May 24, 2011

- One mezzanine has been fully assembled. Two more are partially assembled (without FPGA). Expect to get two XC5VLX110 FPGA by the end of September (20 weeks lead time).

- Both PROMs work perfectly
  - XCF32P
    - 13 min programming time from VCC
    - 116 milliseconds reconfiguration time with 30MHz crystal
  - XCF128X
    - 13 min programming time from VCC
    - 58 milliseconds reconfiguration time with 30MHz crystal

- Can switch between two revisions of the firmware with the XCF128X PROM, as described in Xilinx Application Note XAPP1100

- 9TMB-to-MPC test works as expected, no errors and same “safe window” as with the old FPGA