Update on CSC Endcap Muon Port Card

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- **Track Finder crate in the counting room**
- **Peripheral crate on iron disk (one out of 60)**
- **FED crate in the counting room (one out of 4)**

- **TTC Optical Fibers**
- **Four LVDS links to Global Muon Trigger**
- **Trigger optical links (3 out of 180)**
- **DAQ optical link (one out of 468)**

- **Skewclear copper cables to peripheral crates (10 or 12 per chamber)**

- **Cathode Strip Chamber (one out of 468)**

**SLINK64 to CMS DAQ**
Upgrade Requirements

- Up to 2 Local Charged Tracks (LCT) coming from Trigger Motherboard, each LCT is 32-bit long
- Be able to deliver 12..18 LCTs from the Muon Port Card to Sector Processor (currently, only 3 LCTs out of 18)
- Preserve and even enhance sorting capabilities of the Port Card
- All optical links should fit single Track Finder crate
- Compatibility with the present CSC Track Finder
- Radiation tolerance
Upgrade Path

- Use existing Muon Port Card main board
  - TMB interface remains unchanged (2 LCTs per TMB @ 80MHz)
  - 3 “old” optical links are still available

- Replace only the FPGA mezzanine
  - Use modest Virtex-5 XC5VLC110-1FF1153
  - Virtex-5 I/Os are compatible with the 3.3V MPC interface

- Place the FPGA, 12 Texas Instruments TLK2501 serializers and one SNAP12 parallel optical transmitter on a new mezzanine
  - 12 LCTs @ 80MHz or
  - 18 LCTs @ 120MHz

- Use CERN designed QPLL2 ASIC to obtain low-jitter 80MHz and 120MHz clocks for the TLK2501 serializers
Muon Port Card Block Diagram

MUON PORT CARD

VME INTERFACE

QPLL2  QPLL2
40/80 MHz  120 MHz

FPGA

Mezzanine Board

15 x TLK2501

3 old optical links compatible with the present Sector Processor

SNAP12 Transmitter to new Sector Processor

CCB
TMB1
TMB2
TMB3
TMB4
TMB5
TMB6
TMB7
TMB8
TMB9
winners
Virtex-5 Mezzanine

- Two new mezzanines in hand, assembled in summer 2010
- The other two boards will be assembled by February 2011
Old And New Mezzanines Installed

[Two images of circuit boards]
Firmware Development

- **Major redesign from Virtex-E to Virtex-5**
  - Initially focused on 80MHz design
  - Leave basic features unchanged for software compatibility
  - Upgrade sorter from “3 best LCTs out of 18” to “12 best LCTs out of 18” (add 2 BX latency)
  - Add extra output FIFO buffers to keep 12 best “new” patterns in addition to 3 “old” ones for testing purposes

- **Progress**
  - Project transition from Virtex-E (Xilinx development system ISE 6.2.03) to Virtex-5 (ISE 12.3) took ~2 months, including debugging
  - FPGA is ~30% full
  - Compilation time ~1 hour
Optical Tests
Test Results

- 3 old optical links work well
- New optical links have been checked with the Zarlink 60102 receiver sitting on older evaluation board (with the TLK2501 is a deserializer). No errors with simple patterns and 127–pattern PRBS.
- PRBS test with the Sector Processor board (5 m MTP-LC fiber splitter, 8 channels, BER < 10^-13)
- Data transmission test from 9 TMBs to MPC in the peripheral crate works well.
Present Status and Plans

- Mezzanine draft specification is available at
  http://bonner-ntserver.rice.edu/cms/projects.html#mpcmez
- Firmware development for the 120MHz transmission tests
  is in progress
- Custom 120.236058MHz and 160.314744MHz crystals (per
  CERN specification, same package) have been ordered from
  Micro Crystal in early September. Expect to get 50+50 pcs
  by February 2011.
- Tests with the SNAP12 receiver board (Sector Processor’s
  upgrade prototype), 100 m optical cable, later in February –
  March 2011
- FPGA and EPROM irradiation tests at the Texas A&M
  University cyclotron, spring 2011