Update on Muon Port Card
FPGA Mezzanine Board

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Upgrade Path

- Use existing Muon Port Card main board
  - TMB interface remains unchanged (2LCTs per TMB @ 80MHz)
  - 3 “old” optical links are still available
- Replace only the FPGA mezzanine
  - Use modest Virtex-5 XC5VLC110-1FF1153
  - Virtex-5 I/Os are compatible with the 3.3V MPC interface
  - Even the slowest -1 speed grade seems to be OK (only $1,613/pc)
- Place 12 TLK2501 serializers on the mezzanine
- Place 12-channel SNAP12 transmitter on a small plug-in board
  - Both low- and regular-profile modules can be used
- Use two separate QPLL2 ASICs to obtain low-jitter 80MHz and 120MHz clocks for the TLK2501 serializers
  - 12 LCTs @ 80MHz or
  - 18 LCTs @ 120MHz
Muon Port Card Block Diagram

MUON PORT CARD

VME INTERFACE

QPLL1
QPLL2

40/80 MHz
120 MHz

CCB
TMB1
TMB2
TMB3
TMB4
TMB5
TMB6
TMB7
TMB8
TMB9

winners

3 old optical links compatible with the present Sector Processor

SNAP12 Transmitter to new Sector Processor

FPGA

Mezzanine Board

15 x TLK2501
Virtex-5 Mezzanine (Top)
Virtex-5 Mezzanine (Bottom)
Old And New Mezzanines Installed
SNAP12 Plug-In Transmitter Board

- 10 boards in hand, three assembled
- Two pairs of Zarlink ZL60101/102 transmitter/receiver in hand
Virtex-5 Mezzanine Status

- Three boards in hand
  - Two assembled with FPGA, one partially assembled without FPGA
  - One QPLL and 160.3174MHz oscillator installed (the other QPLL and 120.2379MHz oscillator are not)

- Initial Tests
  - Mechanical compatibility with the main Port Card board and plug-in SNAP12 board
  - Power distribution (1.0V, 1.8V, 2.5V, 3.3V)
  - FPGA/PROM access via Xilinx USB cable
Firmware Development

- Major redesign from Virtex-E to Virtex-5
  - Current focus on 80MHz design
  - Leave basic features unchanged for software compatibility
  - Upgrade sorter from “3 best LCTs out of 18” to “12 best LCTs out of 18” (add 2 BX latency)
  - Add extra output FIFO buffers to keep 12 best “new” patterns in addition to 3 “old” ones for testing purposes

- Progress
  - FPGA is ~30% full; compilation time ~1 hour
  - Data transmission test from 9 TMBs to MPC
  - “Safe window” is about the same as for the old mezzanine, as expected (the width of “safe window” depends mostly on GTLP transmitter/receiver parameters and various propagation delays)
What Is Next

- Check timing (3 “old” and 12 “new” optical links)
- Check 3 “old” optical links with the new data source (V-5)
- Try to debug SNAP12 transmitter with SNAP12 receiver installed on the same plug-in board; use TLK2501 and one of older evaluation optoboards for initial channel-by-channel tests
- Continue firmware development
- Prepare initial specification