Some Technical Details on

- TTCrx ASIC
- TTCrq mezzanine
- CCB2004

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4-bit Trigger Control Commands

6-bit short broadcast and 14-bit long broadcast/individual TTC Commands

• B-Go[3:0] are four signals that arrive from the Local or Central Trigger Controller (LTC & CTC) to the front panel of the TTCci

• B-Go[3:0] specify from which B-Go channel (TTCci FIFO) a particular framed TTC command will be sent out on the TTC B-channel

• B-Go bit assignment is given in Table 5 of the CMS Note 2002-033

• It is a subsystem’s choice on how to decode a 6-bit TTC short broadcast command

• EMU decoding scheme shown in Table 7 of the CCB manual was implemented by all CSC EMU peripheral and TF boards

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From the J. Varela’s CMS Note 2002-033

Table 5: B-Go Commands

<table>
<thead>
<tr>
<th>B-Go channel</th>
<th>B-Go bits</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0001</td>
<td>BC0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reset Bunch crossing counters to begin a new L1C orbit</td>
</tr>
<tr>
<td>2</td>
<td>0010</td>
<td>Test Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>to start calibration procedure</td>
</tr>
<tr>
<td>3</td>
<td>0011</td>
<td>Private Gap</td>
</tr>
<tr>
<td>4</td>
<td>0100</td>
<td>Private Orbit</td>
</tr>
<tr>
<td>5</td>
<td>0101</td>
<td>ReSync</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(=L1Reset) clears buffers and pipelines, etc.</td>
</tr>
<tr>
<td>6</td>
<td>0110</td>
<td>HardReset</td>
</tr>
<tr>
<td>7</td>
<td>0111</td>
<td>Reset Event Counter</td>
</tr>
<tr>
<td>8</td>
<td>1000</td>
<td>Reset Orbit Counter</td>
</tr>
<tr>
<td></td>
<td></td>
<td>normally sent at begin of a new run</td>
</tr>
</tbody>
</table>

From the CCB Specification

Table 7: Fast Control Bus Ceb cmd[5:0] and Ceb data[7:2] (**) Commands

<table>
<thead>
<tr>
<th>Signal</th>
<th>Code (hex)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC0</td>
<td>01</td>
<td>Bunch Crossing Zero</td>
</tr>
<tr>
<td>L1 Reset</td>
<td>03</td>
<td>Reset L1 readout buffers</td>
</tr>
<tr>
<td>Hard reset (**)</td>
<td>04</td>
<td>Reload all FPGAs from EPROMs</td>
</tr>
<tr>
<td>Start Trigger</td>
<td>06</td>
<td></td>
</tr>
<tr>
<td>Stop Trigger</td>
<td>07</td>
<td></td>
</tr>
<tr>
<td>Test Enable</td>
<td>08</td>
<td></td>
</tr>
<tr>
<td>Private Gap</td>
<td>09</td>
<td></td>
</tr>
<tr>
<td>Private Orbit</td>
<td>0A</td>
<td></td>
</tr>
<tr>
<td>CCB hard reset (**)</td>
<td>08</td>
<td>Reload Xilinx FPGA from its EPROM on CCB 2004 board</td>
</tr>
<tr>
<td>TMB hard reset (**)</td>
<td>10</td>
<td>Reload TMB FPGA’s from EPROM</td>
</tr>
<tr>
<td>ALC hard reset (**)</td>
<td>11</td>
<td>Reload ALC FPGA’s from EPROM</td>
</tr>
<tr>
<td>DMB hard reset (**)</td>
<td>12</td>
<td>Reload DMB FPGA’s from EPROM</td>
</tr>
<tr>
<td>MPC hard reset (**)</td>
<td>13</td>
<td>Reload MPC FPGA’s from EPROM</td>
</tr>
<tr>
<td>DMB cfeb calibrate0</td>
<td>14</td>
<td>CFB Calibrate Pre-Amp Gain</td>
</tr>
<tr>
<td>DMB cfeb calibrate1</td>
<td>15</td>
<td>CFB Trigger Pattern Calibration</td>
</tr>
<tr>
<td>DMB cfeb calibrate2</td>
<td>16</td>
<td>CFB Pedestal Calibration</td>
</tr>
</tbody>
</table>
TTCrx Programmable Delays

  - 0..15 BX delay
  - programmable over TTC (write only) or I²C on CCB over VME (R/W)
  - by default set to “0” (not the case for very few boards out of ~100; see next slide for required initialization steps)
  - bits [3:0] must be equal to bits [7:4] for proper command decoding!

- Fine Delay Registers for Clock40Des1 and Clock40Des2
  - 104 pc accuracy (25 ns divided into 240 steps)
  - special encoding (delay is not proportional to register value), see TTCrx manual
  - programmable over TTC (write only) or I²C on CCB over VME (R/W)
  - by default set to “0”
TTCrx Fine Delay Calculation

Conversion formulas

\[ K = \left[ m \cdot 15 + n \cdot 16 + 30 \right] \mod 240, \]
\[ n = K \mod 15, \]
\[ m = \left[ (K \div 15) - n + 14 \right] \mod 16. \]

with \( \div \) denoting the integer division operator (with truncation.)

The values of \( n \) and \( m \) are then combined to an 8-bit value \( nm \)

\[ nm = 16 \cdot n + m, \]

which can be written to one of the Fine Delay registers.

\[
\text{Delay} = K \times 104 \text{ ps}, \text{ where } K = 0..239
\]

(nm) is a value to be written into the fine delay register

For more details and Conversion Table see Appendix A of the TTCrx Manual
TTCrx Fine Delay Measurements

Yellow waveform is Clock40 non-deskewed clock output of the TTCrx ASIC
Blue waveform is Clock40Des1 deskewed clock output of the TTCrx ASIC
Conclusion: good agreement between the measurements and calculations
CCB Clock Settings

- 40.08Mhz clock for all peripheral (TF) boards originates from the QPLL on TTCrx

- 80.16MHz clock for the TLK2501 serializers on MPC originates also from the QPLL

- 40.08MHz Clock40Des1 from the TTCrx ASIC is used as an input for the QPLL
  - soldered jumper on TTCrq mezzanine

- 40.08MHz and 80.16MHz clocks derived from the QPLL work properly only when:
  - TTC fiber is plugged in AND TTCrx is ready AND QPLL is locked
  - “TTC_Ready” and “QPLL_Locked” signals are available for VME read from the CCB
  - These two signals should probably be monitored periodically
CCB/TTCrx Initialization

- The following steps have to be done from the top of the TTC tree:
  - Load pre-defined values into Coarse and Fine Delay registers.  
    Note: Coarse delay register bits [3:0] must be equal to bits [7:4]
  - Enable parallel output bus on the TTCrx (write 3Bh into Control register)
  - Send long-format broadcast command=0 to TTCrx
    (clear the discrete logic decoder on CCB board)

- For more details see “The CCB2004, MPC2004 and MS2005 User’s Guide”
Other TTCrx/CCB Delays

• L1A latency (TTCrx) = 64..83 ns (typ = 71 ns), see TTCrx Manual, Chapter 9

• In the “Discrete Logic” mode all the signals (Command Bus, L1A) arriving from the TTCrq mezzanine are delayed for 2BX on the main CCB2004 board for synchronization before distribution to custom backplane

• In the “FPGA/Internal” mode the broadcast commands are sent from VME and are not delayed

• In the “FPGA/Internal” mode the L1A may originate from several sources (TTC, VME, TMB, front panel, DMB_cfebc_calibrate, ALCT_adb_pulse_sync/async)
  - L1A can be delayed for 1..255 BX (CSRB5[7:0])
  - ALCT and CLCT External Triggers can be delayed for 1..255 BX (CSRB5[15:8])
Individually Addressed TTC Commands

- Can be sent on TTC channel B as well as broadcast commands

- Allow to address individual TTCrx ASICs within a TTC partition

- Each TTCrx has a unique 14-bit ID number encoded with a soldered jumpers on TTCrq mezzanine board (see TTCrx Manual, Chapter 8)

<table>
<thead>
<tr>
<th>SubAddr[5:0]</th>
<th>Data[7:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>13 12 11 10 9 8</td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
</tbody>
</table>

Unique 8-bit ID number

Equal to CCB serial number 1..95 as marked on the front panel

- 6 lowest bits of the unique 8-bit ID numbers are used to form the two I^2C addresses to access the TTCrx ASIC (see TTCrx Manual, Chapter 7)

- 14-bit ID can be read out from CSRB18 (after TTCrx_Reset) or directly from the TTCrx over serial I^2C bus (under VME control)
TTCrx Response to L1A

- After the reception of an L1A on channel A, the TTCrx ASIC outputs sequentially on the 12-bit “Bunch Counter Bus” the contents of the TTCrx internal 12-bit Bunch Counter and 24-bit Event Counter. Counters are set to “0” on BCntRes and EvCntRes broadcast commands respectively.

- These values are latched into CSRB[12:14] and available for read over VME. Also they can be read out (but much slower) from the TTCrx over I²C bus.
CCB, MPC, MS User’s Guide

• Companion document to CCB2004, MPC2005 and MS2005 specifications

• Comprehensive 38-page (version 1.4) User’s Guide on:
  - Board initialization
  - Step-by-step programming in various modes
  - Instructions on how to run the chain tests
  - Firmware downloading
  - Updated pin assignment for all slots in the peripheral and TF crates

• Available at http://bonner-ntserver.rice.edu/cms/users_guide_14.pdf