CSC Electronics Upgrade

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CSC Electronics

Track Finder crate in the counting room
Peripheral crate on iron disk (one out of 60)
FED crate in the counting room (one out of 4)

TTC Optical Fibers

Four LVDS links to Global Muon Trigger

Trigger optical links (3 out of 180)

DAQ optical link (one out of 468)

Skewclear copper cables To peripheral crates (10 or 12 per chamber)

Cathode Strip Chamber (one out of 468)

SLINK64 to CMS DAQ
Peripheral Crate and Backplane
Track Finder Crate and Backplane
Xilinx FPGA on CSC Trigger Boards

On-chamber
- Anode LCT Boards (3 types)

Peripheral Crates
- Trigger Motherboard
- Muon Port Card

Track Finder
- Sector Processor
- Muon Sorter

Virtex-E (2001)
Virtex-2 (2005)


Virtex-5 (2009)
Virtex-2 (2005)
Phase 1 Upgrade (EMU)

- Build and install 72 ME4/2 chambers

- Replace 360 ME1/1 Cathode Front End Boards (CFEB) with Flash ADC Digital version DCFEB (OSU). Move current CFEBs to ME4/2.

- Design new Trigger Motherboard (TMB), DAQ Motherboard (DMB) and Low Voltage Distribution Board (LVDB) for ME1/1 to match DCFEB optical links and power requirements and improve processing capabilities
Phase 1 Trigger Upgrade Plans

- Keep limit of 2 LCT/chamber/BX
- Stay within 3.1 us latency
- Use existing peripheral backplane
- Upgrade TMB only for ME1/1 (72) \(\rightarrow\) TAMU & UCLA
  - Avoid system-wide upgrade of ALCTs (540) and TMB (540)
- Upgrade Muon Port Card (60 total) \(\rightarrow\) Rice
- Upgrade Sector Processor (12 total) \(\rightarrow\) Florida
- Upgrade Muon Sorter (1) \(\rightarrow\) Rice
- Evolutionary approach: introduce new components in parallel with existing system
Muon Port Card Upgrade (1)

- Currently selects 3 best LCTs out of 18 and transmits them to Sector Processor, but will need to select more for higher occupancy
- Additional sorting and faster links
- Current sorting scheme is very efficient and flexible. Can be easily upgraded to “n out of 18”. Simulation shows only ~15% increase in logical resources for “7 out of 18” and 1BX extra latency for two LCTs to be sorted
Muon Port Card Upgrade (2)

- Present optical links to CSC Track Finder run at 1.6Gbps (one link per LCT)

- 16-bit @ 80Mhz from FPGA
- TI TLK 2501
- Finisar FTRJ 8519

- 16-bit @ 80Mhz to FPGA
- TI TLK 2501
- Xilinx Virtex-2 FPGA

- 50/125 um multimode fiber
- 59..113 m long

- 2x5 SFF optical transceiver
- 1.6 Gbps simplex transmission

- 16-bit SERDES
- 8B/10B encoding
- 82ns average latency @80MHz (SER + DESER)
- PRBS capability
- Will need to increase throughput up to 9.6Gbps to be able to transmit up to 18 LCTs from one peripheral crate to TF

![Diagram of FPGA and Muon Port Card with links A and B]

- 3 x 1.6Gbps (old links)
- 3 x 9.6Gbps (new links)
Phase 1 Trigger R&D

- Conceptual Design of the CSC Track Finder (evolution of existing model, 1 crate)
- Evaluation of the most advanced Xilinx FPGA (Virtex-6)
- Evaluation of Gbps data communication links and serdes
- Evaluation of uTCA technology for track-finding processing
- Prototypes associated with above
Phase 2 Trigger Plans

- Stay within an increased latency of 6.2 us
- Adapt to new TTC system
- Combined CSC-Tracker trigger to improve trigger performance
- New Clock and Control Board (61 total, same board for all peripheral and Track Finder crates) → Rice
- Further upgrade of CSC electronics (all TMBs and DMBs)?
- Track Finder outputs to Tracker-matching Trigger