Databus Systems in High Energy Physics (HEP): Past, Present, and Future

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January 28, 2008
• What is Databus System
• Legacy Standards
  - NIM
  - CAMAC
  - FASTBUS
  - Multibus and Multibus-2
• Modern Standards
  - VME/VME64/VME64x, VXI
  - CompactPCI (cPCI), PXI
• Next Generation Standards
  - Switch Fabrics
  - cPCI Express, VITA 31, VITA 41, VITA 46, VITA 48
  - ATCA and MicroTCA
• Applications in HEP Experiments: Few Examples
  - CDF at Fermilab
  - CMS at CERN
  - International Linear Collider
• Databus Market: Current State and Perspectives
• Conclusion
What is Databus System?

Databus Specification defines:

- **Electrical interface** (drivers, receivers, power…)
- **Logical communication** (addressing, data exchange protocol, multiprocessing, interruptions…)
- **Mechanical implementation** (connectors, crate, rack…)

Databus Milestones

NIM, 1964

CAMAC, 1969

VME 6U, 1981

FASTBUS, 1986

VME 9U, 1994

CompactPCI, 1995
HEP Community was a driving force of databus development in early 60’s
- Physicists needed to collect data (mostly high speed readout) from thousands of identical or similar data channels within relatively small experimental areas
- Accelerator people needed to remotely control accelerator equipment (mostly bidirectional transfers at lower rates, but longer distances)
- Early computers did not have enough input/output capabilities to accept/send such amounts of data from/to unique equipment
- Databus provided an intermediate level of data readout, buffering and simple preprocessing between custom detector electronics and commercial data acquisition and control computers

Every large HEP laboratory has a pool of hardware (crates, power supplies, functional modules, cables) available for on-site users
Nuclear Instrument Module (NIM)

Pin No. | Function
--- | ---
10 | +6 V
11 | -6 V
16 | +12 V
17 | -12 V
28 | +24 V
29 | -24 V
34 | Power Return Ground
33 | 117 V ac, hot
41 | 117 V ac, neutral
42 | High Quality Ground
NIM is actually NOT a databus: there is no common backplane bus.

- Backplane provides only powers to functional modules.
- 250 x 193 mm board size, 12 boards per crate maximum.
- Plug-and-play approach (does not need any software!)
- Amplifiers, shapers, discriminators, delay units etc.
- Front panel settings and cable connections.
- IEEE-488 (GPIB) cable bus was envisaged to control individual modules, but in practice rarely used.
Computer Aided Measurement and Control (CAMAC)

- **IEEE 583 Crate level standard**
  - 25 stations in the crate
  - 1 crate controller
  - Access modules using CNAF function
    - C: Crate Number 1-7;
    - N: Station Number 1-25;
    - A: Address 0-15;
    - F: Function 0-31;
  - 1 microsecond data exchange cycle

- **IEEE 596 Parallel Highway Interface (Parallel CAMAC)**
  - Up to 7 crates
  - 24-bit wide data transfers @ 1MHz
  - Twisted pair cable bus, up to 15 m

- **IEEE 595 Serial Highway Interface (Serial CAMAC)**
  - Up to 62 crates
  - 1-bit serial and 1-byte wide data transfers
  - Twisted pair cable bus, up to 2 km
CAMAC History

- CAMAC was the first successful databus interface between commercial computers and custom detector electronics
- Most of physics experiments in late 60’s – late 80’s were based on parallel CAMAC electronics
- Several large distributed accelerator control systems (CERN, Fermilab) were based on serial CAMAC

But:

- CAMAC is slow (both parallel and serial buses)
- Board size is relatively small, especially for multi-channel electronics
- Backplane interface takes significant amount of board space
- Limited support of multiprocessing
- Not suitable for demanding analog requirements because of high noise of digital circuits
- Hard to build large multi-crate systems

CAMAC has inspired the development of FASTBUS in late 70’s
FASTBUS Features

- ANSI/IEEE 960-1986 Standard
- Large 367 x 400 mm board
- 26 slots in crate
- ECL backplane signals
- Asynchronous transfers
- 32-bit data/32-bit address
- 100 ns cycle
- Up to 160Mbyte/s bandwidth
- Multiprocessing
- Block transfers
- Sparse data scanning
- Well defined control and status registers

But:
- High power consumption
- Poor backplane connector
- Complex intercrate interface
- Weak industry support
FASTBUS History

- FASTBUS was widely used in late 80’s – mid 90’s in HEP community:
  - CDF Run I (1985-1995): ~1500 modules in ~150 crates
  - All four experiments at the LEP e+e- collider at CERN (DELHI, ALEPH, L3, OPAL) in 1989-2000: ~700 crates
  - At SLAC, DESY and other smaller experiments

- 20,000 to 30,000 total estimated number of FASTBUS boards of few hundred types produced in the world

- Lower cost per channel for multi-channel boards (ADC, TDC) comparing to CAMAC

- FASTBUS was the last general purpose databus system developed and designed by HEP community. It turned out that it is more efficient approach to adopt existing commercial solutions, including databuses, to physicists’ needs rather than design new hardware from scratch.
Board Height, U
Table:

<table>
<thead>
<tr>
<th>Board Height, mm (“”)</th>
<th>3U</th>
<th>6U</th>
<th>9U</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 mm (3.937”)</td>
<td>233.35 mm (9.187”)</td>
<td>366.7 mm (14.437”)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Board Length</th>
<th>3U</th>
<th>6U</th>
<th>9U</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 mm (3.937”)</td>
<td>160 mm (6.299”)</td>
<td>220 mm (8.661”)</td>
<td>280 mm (11.024”)</td>
</tr>
<tr>
<td>160 mm (6.299”)</td>
<td>220 mm (8.661”)</td>
<td>340 mm (13.386”)</td>
<td>400 mm (15.748”)</td>
</tr>
</tbody>
</table>
Multibus and Multibus-2

**Multibus (1978)**
- Based on Intel 8086 external bus signals
- 60-pin and 86-pin card edge connectors
- 16-bit data/24-bit address

**Multibus-2 (1984)**
- Processor independent
- 32-bit multiplexed address/data bus
- Synchronous data exchange protocol
- Euromechanics, 233 x 220 mm board

Intel’s Multibus and Multibus-2 were successful in industry, but found only limited use for accelerator control in HEP.

Both Multibus and Multibus-2 were defeated by VME in late 80’s – early 90’s during “bus war” and completely disappeared since then.
VersaModule Eurocard (VME) standard was proposed in 1981 by Motorola, Mostek and Signetics
Processor independent, but signal set has its roots in MC68000 CPU
Open architecture; 50,000 copies of the initial VME specification were sent out free of charge to gain attention and attract developers and users
VME International Trade Association (VITA) remains the driving force
VME Features

- 2-21 slot backplanes available
- 3-row 96-pin DIN 41612 connectors
- Press-fit sockets on the backplane
- Terminators on both ends of the backplane for bussed signals
- Asynchronous protocol
- Up to 40Mbyte/s bandwidth

Mandatory bus for all 3U and 6U boards

Extension bus for A32D32 6U boards

- D<15:0> 16-bit Data Bus
- 24-bit Address Bus
- AM<5:0> 6-bit Address Modifier Bus
- 7 Interrupts
- Arbitration Bus
- Clock, Control and Status signals
- +5V, +12V, -12V powers, 5 GND lines

- D<31:16> 16-bit Data Bus Extension
- A<31:24> 8-bit Address Bus Extension
- Additional +5V (3 lines) and GND (4 lines)
- 64 unbussed User I/O lines
VME Operations

Data Transfer

DS*  
Data Bus  
DTACK*

Data Valid
Data Accepted

IACK
Address Bus
AM Codes
AS*

Address Valid
AM0 – AM5

Times are minimum
Seen from Master

IACK
Address
AM code
AS*

IACK
Address
AM code

IACK
Address
AM code

Data Cycle

Block Cycle

### VME Evolution

<table>
<thead>
<tr>
<th>ANSI/VITA 1.0</th>
<th>VME64 Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSI/VITA 1.1</td>
<td>VME64 Extensions</td>
</tr>
<tr>
<td>ANSI/VITA 1.3</td>
<td>9U x 400 mm Format</td>
</tr>
<tr>
<td>ANSI/VITA 1.5</td>
<td>2eSST</td>
</tr>
<tr>
<td>ANSI/VITA 1.6</td>
<td>Keying for Conduction-cooled VME</td>
</tr>
<tr>
<td>ANSI/VITA 1.7</td>
<td>Increased Connector Current Level</td>
</tr>
<tr>
<td>ANSI/VITA 23</td>
<td>VME64x Extensions for Physics</td>
</tr>
</tbody>
</table>

### VME64 (1994):
- Electrical and mechanical superset of the original IEEE 1014-1987
- 64-bit address and data cycles for 6U boards (use 32-bit address and 32-bit data paths in both address and data cycles)
- 32-bit data and 40-bit address cycles for 3U boards
- Twice the bandwidth of original VME (up to 80Mbyte/s)
- Automatic “plug-and-play” features
- New 160-pin 5-row connector compatible with the original DIN 41612
- Additional 5-row 95-pin metric J0/P0 connector: more inputs/outputs
- Ten +3.3V power pins on row D of J1/P1
- Geographical addressing in the crate
- Bandwidth doubled to 160Mbyte/s due to two edge 2eVME protocol
Further VME Improvements

- **VITA 23 (VME International Physics Association, VIPA)**
  - Better grounding and shielding
  - Sparse data readout
  - Block Transfers
  - Additional supply voltages
- **2eSST (Two edge Source Synchronous) protocol**
  - Data transfer on both edges of synchronization signal without acknowledgement
  - Up to 320Mbyte/s bandwidth, but need special drivers/receivers
- **Increased current per contact**

<table>
<thead>
<tr>
<th>VOLTAGE \ /</th>
<th>VME</th>
<th>VME64</th>
<th>VME64x / VITA 1.7</th>
<th>VME</th>
<th>VME64</th>
<th>VME64x</th>
<th>VITA 1.7</th>
<th>VME</th>
<th>VME64</th>
<th>VME64x / VITA 1.7</th>
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<tbody>
<tr>
<td>+5V / VPC</td>
<td>1</td>
<td>1</td>
<td>1.25</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td>6</td>
<td>6</td>
<td>11.25</td>
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<td>30</td>
<td>30</td>
<td>56.25</td>
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<tr>
<td>+12V</td>
<td>1</td>
<td>1</td>
<td>1.25</td>
<td>2</td>
<td>1</td>
<td>1.25</td>
<td>2</td>
<td>12</td>
<td>12</td>
<td>15</td>
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<td></td>
<td></td>
<td>24</td>
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<tr>
<td>-12V</td>
<td>1</td>
<td>1</td>
<td>1.25</td>
<td>2</td>
<td>1</td>
<td>1.25</td>
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<td>12</td>
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<td>24</td>
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<tr>
<td>+5V Stdby</td>
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<td>1</td>
<td>1.25</td>
<td>2</td>
<td>1</td>
<td>1.25</td>
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<td>5</td>
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<td>+3.3V</td>
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<td>1.25</td>
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<td>12.5</td>
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<td></td>
<td></td>
<td>66</td>
</tr>
<tr>
<td>+V1 (48V optional)</td>
<td>1.25</td>
<td>2</td>
<td>1.25</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>60</td>
<td>96</td>
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<tr>
<td>-V1 (48V optional)</td>
<td>1.25</td>
<td>2</td>
<td>1.25</td>
<td>2</td>
<td></td>
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<td></td>
<td></td>
<td>60</td>
<td>96</td>
</tr>
<tr>
<td>+V2 (48V optional)</td>
<td>1.25</td>
<td>2</td>
<td>1.25</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>60</td>
<td>96</td>
</tr>
<tr>
<td>-V2 (48V optional)</td>
<td>1.25</td>
<td>2</td>
<td>1.25</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>60</td>
<td>96</td>
</tr>
</tbody>
</table>
Established in 1987 on the basis of VME for test and measurement applications

- 1.2” slot spacing (vs 0.8” in VME) limits the number of slots to 13 (vs 21 in VME), but provides more space for mezzanine boards and EMI shielding
- Four form factors, Types C and D are most popular
- Unused contacts of J2/P2 and J3/P3 VME connectors are specified for module identification, triggering, synchronization, clocking, analog summing and additional powers, so the VXI is only partially compatible with VME
CompactPCI is a PCI bus in “Euromechanics” with several additional signals, including geographical addressing:

- 3U x 160 mm and 6U x 160 mm boards
- 2 mm press-fit 5-row connectors
- Pins on the backplane, sockets on board (opposite to VME)
- J1 for 32-bit PCI bus, J2 for 64-bit PCI bus extension, J3/J4/J5 for user IO
- Keying mechanism to distinguish between the +5V and +3.3V boards
- Software compatible with the PCI
CompactPCI Card
CompactPCI Timing

![CompactPCI Timing Diagram]

**cPCI Disadvantages:**
- Small board (3U x 160 mm or 6U x 160 mm)
- Limited power consumption (less than 50W with air cooling)
- Limited number of slots (8) on a segment, need bridges for extension
- Established in 1998 on the basis of the cPCI standard for test and measurement applications
- A subset of VXI signals on J2/J3/J4 connectors
- Up to 8 slots on one segment (same as cPCI)
- Two form factors 3U x 160 mm and 6U x 160 mm (same as cPCI)
## VXI and PXI Comparison

<table>
<thead>
<tr>
<th></th>
<th>VXI</th>
<th>PXI</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data Bus, bits</strong></td>
<td>8, 16, 32</td>
<td>8, 16, 32, 64</td>
</tr>
<tr>
<td><strong>Throughput, Mbyte/s</strong></td>
<td>40 (VME); 80 (VME64); 160 (with 2eVME protocol)</td>
<td>132; 264</td>
</tr>
<tr>
<td><strong>Power, V</strong></td>
<td>+5, -5.2, -2, +12, -12, +24, -24</td>
<td>+3.3, +5, +12, -12</td>
</tr>
<tr>
<td><strong>Board Dimensions, mm</strong></td>
<td>160x100, 160x233, 340x233, 340x367</td>
<td>160x100, 160x233</td>
</tr>
<tr>
<td><strong>Maximum number of slots</strong></td>
<td>13</td>
<td>8</td>
</tr>
<tr>
<td><strong>EMI Board Shielding</strong></td>
<td>Defined in the specification</td>
<td>Module Specific</td>
</tr>
<tr>
<td><strong>Local Bus, lines</strong></td>
<td>12</td>
<td>13</td>
</tr>
<tr>
<td><strong>Trigger Bus, lines</strong></td>
<td>8 TTL + 2 ECL</td>
<td>8 TTL</td>
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<tr>
<td><strong>Clock and Synchronization Signals</strong></td>
<td>CLK10MHz (all sizes), CLK100MHz (size D), SYNC100MHz (size D), all differential ECL</td>
<td>10MHz, TTL (all sizes)</td>
</tr>
<tr>
<td><strong>Cost</strong></td>
<td>Medium-High</td>
<td>Low-Medium</td>
</tr>
<tr>
<td>Databus</td>
<td>CAMAC</td>
<td>Fastbus</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>---------------------</td>
<td>--------------------</td>
</tr>
<tr>
<td>Protocol</td>
<td>Synchronous</td>
<td>Asynchronous</td>
</tr>
<tr>
<td>Data, bits</td>
<td>24</td>
<td>32</td>
</tr>
<tr>
<td>Address, bits</td>
<td>5</td>
<td>32</td>
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<tr>
<td>Address/Data Multiplexing</td>
<td>No</td>
<td>No</td>
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<tr>
<td>Maximum number of boards in crate</td>
<td>25</td>
<td>26</td>
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<tr>
<td>Multiprocessing</td>
<td>Limited</td>
<td>Yes</td>
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<tr>
<td>Logic Levels</td>
<td>TTL</td>
<td>ECL</td>
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<tr>
<td>Number of interrupts</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Databus cycle</td>
<td>1 microsecond</td>
<td>100 ns</td>
</tr>
<tr>
<td>Connector</td>
<td>86-pin card edge type</td>
<td>130-pin</td>
</tr>
<tr>
<td>Board Dimensions, mm</td>
<td>183x285</td>
<td>367x400</td>
</tr>
</tbody>
</table>
Traditional parallel databuses (VME, cPCI) have reached their performance limits at a level of ~66MHz.

A set of point-to-point serial gigabit links is an alternative data path in modular backplane systems.

Switch is a key element to provide flexible connectivity.

Existing semiconductor technologies (embedded gigabit transceivers in the FPGA’s and ASIC’s) support gigabit links.

RapidIO, 10G Ethernet, InfiniBand, StarFabric and PCI Express are the most popular switch fabrics.

2.5Gbps is a typical serial data rate and 10Gbps and higher rates are targets.
VITA 31.1 combines VME64x with Gigabit Ethernet based high speed switch fabric interface.

- Uses PICMG 2.16 cPCI Packet Switched Backplane standard on P0 connector.
- J0/P0 pinout is the same as J3 in the PICMG 2.16 specification.

Example of a 21-slot VITA 31.1 backplane with two fabric (Ethernet switch) slots and 19 node slots for VME boards.
Payload Cards are compatible with VME64x J1/P1 and J2/P2 connectors
- Special Tyco MultiGig RT2 J0 connector for serial links (up to 6.25Gbps).
  Incompatible with the VME J0/P0 connector.
- MultiGig RT2 connector provides 30 serial pairs; 16 are defined in VITA 41
- Switch Cards have 5 Tyco MultiGig RT2 connectors; incompatible with VME64x
VITA 46 (VPX)

- VITA 46 (VPX) uses Tyco MultiGig RT2 connectors only
- 3 connectors P0-P2 of 2 types for 3U boards
- 7 connectors P0-P6 of 2 types for 6U boards
- VMEbus signals are routed on P2 and partially on P3-P5
- Incompatible with VME64x, but hybrid backplane solves the problem
- 32 high speed serial signal pairs
- Much more User I/O pins than in VITA 41
- VITA 48 is a ruggedized version of VITA 46 with more space between boards

- Slots 1-5 are VME64x compatible
- Slots 6-10 are VPX compatible
VME64x, VITA 46 and VITA 48 Boards

VITA 48 Board Assembly

VITA 48 is ruggedized version of VITA 46

# VME64x, VITA 46 and VITA 48 Comparison

<table>
<thead>
<tr>
<th></th>
<th>VME64x</th>
<th>VITA 41 (VXS)</th>
<th>VITA 46 (VPX)</th>
<th>VITA 48 (VPX-REDI)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bandwidth</strong></td>
<td>VMEbus: 320MBytes/s</td>
<td>VMEbus: 320MBytes/s, 16 serial pairs @ 5Gbps</td>
<td>VMEbus: 320MBytes/s, 32 serial pairs @ 10Gbps</td>
<td>VMEbus: 320MBytes/s, 32 serial pairs @ 10Gbps</td>
</tr>
<tr>
<td><strong>Switch fabric configurations</strong></td>
<td>No</td>
<td>Star, Dual Star, Mesh, Daisy Chain</td>
<td>Star, Dual Star, Mesh, Daisy Chain</td>
<td>Star, Dual Star, Mesh, Daisy Chain</td>
</tr>
<tr>
<td><strong>Number of User I/O pins</strong></td>
<td>205</td>
<td>110 + 32 serial + 31 reserved</td>
<td>272 + 64 serial</td>
<td>272 + 64 serial</td>
</tr>
<tr>
<td><strong>Plug-in Unit Pitch</strong></td>
<td>0.8”</td>
<td>0.8”</td>
<td>0.8”</td>
<td>1.0”</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>5V: 90W; 3.3V: 66W</td>
<td>5V: 90W; 3.3V: 66W</td>
<td>5V: 80W; 12V: 384W or 48V: 768W</td>
<td>5V: 80W; 12V: 384W or 48V: 768W</td>
</tr>
<tr>
<td><strong>Cooling</strong></td>
<td>Air</td>
<td>Air</td>
<td>Air</td>
<td>Air, fluid</td>
</tr>
</tbody>
</table>
CompactPCI Express (2005): Switch Fabric on cPCI

- Replaces cPCI J1 and J2 connectors (parallel bus) with four connectors:
  - XP1 Universal Power Module
  - XJ2 and XJ3 for high speed (2.5Gbps) differential serial links
  - XJ4 multifunctional 2mm connector
- J3/J4/J5 connectors on 6U boards remain user defined

Hybrid cPCI Express Backplane
Advanced TeleCommunication Architecture (ATCA)

- PICMG 3.0 ATCA Core specification (2003) and several 3.x specs for RapidIO, 10G Ethernet, InfiniBand, StarFabric, PCI Express, and PRS switch fabrics
- 8U (322 x 280 mm) board, up to 16 slot backplane
- 1.2” (30.48 mm) spacing between boards for better cooling and mezzanines
- High power consumption (up to 200W) per board
- High speed Tyco/ERNI ZD connectors for differential signaling (up to 5Gbps)
- Redundancy at several levels (switch fabrics, power distribution, control)
- Intended for high availability (99.999% readiness) applications
MicroTCA (2006)

- MicroTCA is based on PICMG AMC.0 mezzanine standard for the ATCA
- Two different board sizes (74 x 182 mm and 149 x 182 mm)
- Up to 14 slot backplane
- 170-pin card edge connector
- Complementary to ATCA at a lower cost for the same high availability market
CDF and DZero Experiments at Fermilab

CDF: In operation since 1985
DZero: In operation since 1992
FASTBUS electronics (Run I) was completely replaced with the VME for Run II

- ~750K data channels
- 125 VIPA 9Ux400 mm crates, ~1700 modules of 60 types
- 60 VME 6U crates, ~700 modules
- ~1000 transition cards
- ~25K mezzanine cards
27 km underground tunnel houses:

- In 1989-2000: 90-210 GeV e+e- LEP collider with 4 experiments (DELPHI, ALEPH, L3, OPAL)
- In 2007-20??: 14TeV pp LHC collider with 4 experiments (CMS, Atlas, LHCb, Alice)
Triggering at the CMS Experiment at CERN

- **Level 1**
  - Calorimeter and Muon info
  - 3.2 us latency
  - Custom hardware based

- **Level 2 (High Level Trigger)**
  - 10 ms latency
  - Software based
    (farm of commercial CPU)
EMU Trigger and DAQ Electronics at the CMS (1)

Track Finder crate in the counting room

Peripheral crate on iron disks (one out of 60)

FED crate in the counting room (one out of 4)

~ 16K electronic boards of 20 types
~ 7K FPGA on 4K boards

Trigger optical links (3 out of 180)

DAQ optical link (one out of 468)

Skewclear copper cables to peripheral crates (10 or 12 per chamber)

Four LVDS links to Global Muon Trigger

Cathode Strip Chamber (one out of 468)
EMU Trigger and DAQ Electronics at the CMS (2)

- VMEbus is used for testing, downloading and calibration purposes only
- Data readout and triggering are performed through dedicated paths:
  - Skewclear cables from on-chamber electronics to peripheral EMU crates
  - Custom backplanes in the peripheral crates
  - Optical links from peripheral crates to Track Finder (TF) and DDU crates in the underground counting room
  - Custom backplanes in the TF and DDU crates
  - Dedicated links from the TF to Global Muon Trigger and from the DDU crates to data processing farm
International Linear Collider (ILC)

- Next Generation (mid 21\textsuperscript{st} century) e+e- collider (Europe, Japan or USA)
- 500 GeV @ 30 km at a first stage, 1 TeV @ 50 km at a second stage
- Estimated amount of equipment:
  - 18,000 RF cavities
  - 17,000 magnets with power supplies
  - 10,000 vacuum pumps
  - 3,000 beam monitors
ATCA and MicroTCA for the International Linear Collider

- Proposed architecture of the ILC control system is based on ATCA and MicroTCA. Evaluation is in progress since 2005.
- Estimation for the Main Linac:
  - 2,000 ATCA crates
  - 25,000 ATCA boards with 4 MicroTCA mezzanines each
VME was a success due to VME/VME64/VME64x backward compatibility
By 2008 VME market approaches $1B and ~50% of applications are military
By 2008 cPCI market approaches $400M and ~70% of applications are telecom

VXI market approaches $800M and remains stable
PXI market approached $200M in 2006 and continues to grow (as a cheaper alternative to VXI)
New switch fabric technologies are incompatible with two main predecessors (VME and cPCI), but hybrid solutions provide a bridge
ATCA and MicroTCA market exceeded $500M in 2007 and may approach $1B in 2008; targets telecom applications; ATCA and uTCA are to replace cPCI.
Conclusion

- NIM is alive and still in use (no databus and no software required!)
- CAMAC is obsolete
- Multibus, Multibus-2 and FASTBUS are now completely dead
- VME is 27 years old, but still strong and has potential for another 27 years. Favorite bus in physics community.
- CompactPCI is popular in industry and competes with VME in many areas. However, it is much less used in HEP community because of smaller board and short backplane.
- Proliferation of serial switch fabrics in various forms continues. ATCA and MicroTCA have strong potential, including future HEP experiments.
- Physicists do not invent databuses any more. Instead, they used to adopt commercial databus products and components for their needs and/or build custom electronics that complies with industry standards.