Muon Port Card Upgrade

M. Matveev
Rice University
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CSC Electronics

Track Finder crate in the counting room

Peripheral crate on iron disk (one out of 60)

FED crate in the counting room (one out of 4)

TTC Optical Fibers

Four LVDS links to Global Muon Trigger

Trigger optical links (3 out of 180)

DAQ optical link (one out of 468)

Skewclear copper cables To peripheral crates (10 or 12 per chamber)

Cathode Strip Chamber (one out of 468)

SLINK64 to CMS DAQ
Outline

- **Sorter Upgrade (N>3)**
  - FPGA resources
  - Latency

- **Optical Links to Track Finder**
  - GBT + Versatile Link
  - QSFP (Quad Small Form-factor Pluggable)
Sorter ‘3 best LCTs out of 18’
Sorter “N best LCTs out of 18”
FPGA Functionality for N=7

FPGA

VME

From TMB1

From TMB2

From TMB9

CSR[0][1]

CSR[0][1]

CSR[0][1]

FIFO_A1

FIFO_A2

FIFO_A9

MUX

MUX

MUX

FIFO_B1

FIFO_B2

FIFO_B3

FIFO_B4

FIFO_B5

FIFO_B6

FIFO_B7

LCT_1

LCT_2

LCT_3

LCT_4

LCT_5

LCT_6

LCT_7

TO SP

TO SP

TO SP

TO SP

TO SP

TO SP

TO SP

“Winner” Bit Encoder

“Winner” bits to TMB1-TMB9

SORTER “7 OUT OF 18”
Simulation Results (7 out of 18)

- 18 LCTs from 9 TMBs
  - 2 frames @ 80MHz

- Best selected LCTs
  - 3 out of 7 shown,
  - 2 frames @ 80MHz

- Winner bits,
  - all 7 shown,
  - 2 frames @ 80MHz
Sorter “7 LCTs out of 18”

- Expanded version of the present sorter “3 out of 18 LCTs”
- Requires only ~15% more logical resources of the FPGA
- Fits into present XCV600E-8FG680 FPGA well (with the exception of additional 64 outputs)
- Adds only 2 BX latency; may be reduced in the future FPGA
- Algorithm has been tested in the MPC2004 with a limited number of patterns from FIFO_A[18:1] passing through the sorter and stored in FIFO_B[7:1]
MPC-to-SP Optical Link

- 16-bit @ 80Mhz from FPGA
  - Xilinx Virtex-E FPGA
  - TI TLK 2501
  - Finisar FTRJ 8519

- 16-bit @ 80Mhz to FPGA
  - Finisar FTRJ 8519
  - TI TLK 2501
  - Xilinx Virtex-2 FPGA

- 50/125um multimode fiber
- 51..112m long
- 2x5 SFF optical transceiver
- 1.6 Gbps simplex transmission
- 16-bit SERDES
- 8B/10B encoding
- 82ns average latency @80MHz (SER + DESER)
- PRBS capability

Muon Port Card

SP 1..12

180 optical links total
48 copper links total
CERN GBT Link

- GBTX Parallel bus mode
  - 80 bits @ 40MHz or
  - 40 bits @ 80MHz
- Present LCT format:
  - 16 bits @ 80MHz
- One GBT link is good for 2.5 LCTs

GBTX – CERN Designed Gigabit Transceiver ASIC
GBLD – CERN Designed Gigabit Laser Driver
GBTIA – CERN Designed Transimpedance Pre-Amplifier and Limiting-Amplifier
DESER – Embedded Deserializer
QuadSFP Optical Link

- QSFP Industry Standard
- Pluggable 4-channel Transceiver
- Up to 5Gbps per channel
- Direct connection to FPGA serial gigabit links
- 38-pin connector
- 12 QSFP transceivers may fit the front of 9U board
Conclusion

- Modest increase in logical resources for N>3 sorted LCTs
- ~1BX latency increase for extra 2 sorted LCTs
- Peripheral GTLP backplane is close to its limits (80MHz)
- Latencies:
  - Texas Instruments TLK2501/3101: Tx: 1.5-2T, Rx: 4-5.5T
  - Xilinx Virtex-2Pro: Tx: 14-19T (TXUSRCLK), Rx: 25-42T (RXUSRCLK)
  - Xilinx Virtex-5LXT: Tx: 4-9.5T (TXUSRCLK), Rx: 8.5-13.5T (RXUSRCLK)
  - GBTX: Tx: 2-3T, Rx: 2-3T, Rx FPGA Core: ???
- Max number of optical links from one MPC to Sector Processor (for 32-bit LCT@40MHz):
  - 9 @ 3.2Gbps
  - 6 @ 4.8Gbps
  - 3 @ 9.6Gbps [Currently 3 @ 1.6Gbps]