CMS EMU Muon Port Card

Draft Specification

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Introduction

In each of stations 2-4 of the Cathode Strip Chambers at the CMS Experiment, the Muon Port Card (MPC) receives trigger primitives (LCT) from nine chambers corresponding to 60 degree sectors. Each MPC in these regions reduces the number of LCTs to three and sends them over optical links to Sector Processor (SP) [1] module residing in the Track Finder (TF) crate. In station 1, an MPC receives LCT's from eight chambers corresponding to 20 degree sectors. For these regions the number of selected LCT's is two. An MPC's will reside in the middle of the 21-slot 9U*400 mm VME crates located on the periphery of the return yoke of the CMS detector. Other slots in a crate will be occupied by the TMB boards [2] (9 or 8 total), DAQ Motherboards [3] (9 or 8 total), Clock and Control Board (CCB) [4] and VME Master [5]. The CCB is the main interface to CMS Trigger, Timing and Control (TTC) System. The VME Master performs the overall crate monitoring and control. All trigger/DAQ modules in a crate will communicate with each other over custom backplane residing below VME P1 backplane. An MPC block diagram is shown on Fig.1. It includes an interfaces to VME, CCB and TMB's, the main processing unit located on a mezzanine card, three data serializers and three optical transmitters.

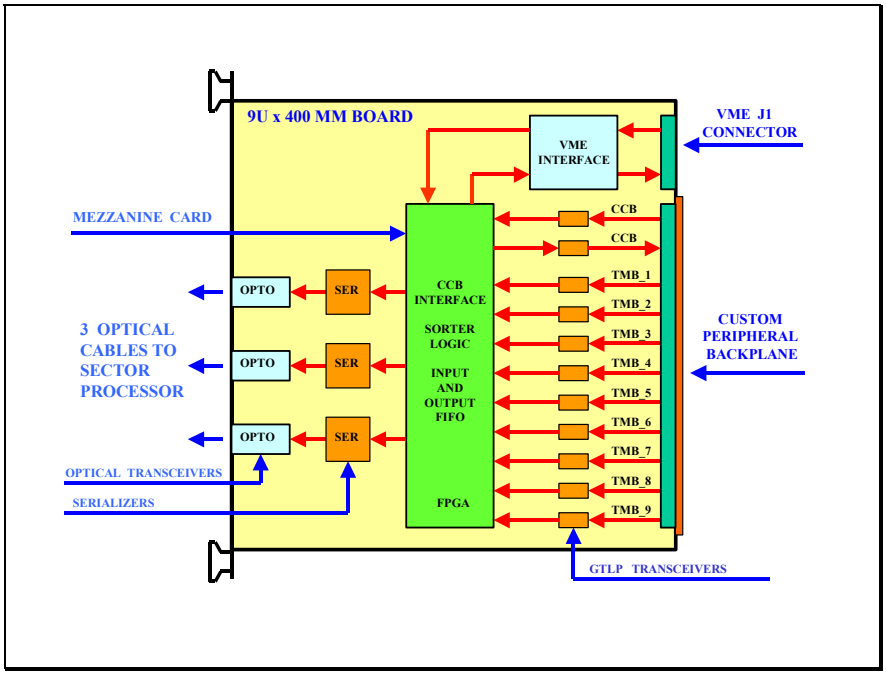

Fig.1: Muon Port Card Block Diagram

1. Interface to Clock and Control Board

The CCB distributes several common (bussed) and individual (point-to-point) signals to each module in the peripheral crate. A full list of these signals is given in [4]. Its subset relevant to MPC that comprises 32 signals is shown in Table 1. 40Mhz clock signal from CCB is distributed over LVDS lines. All the rest signals are transmitted using GTLP logic standard, with active level "0". The list of commands decoded by the MPC from the ccb_cmd[5..0] lines is shown in Table 2.

Table 1

CCB-to-MPC Signals

Signal	Bits	Type	Logic	Duration
Ccb_clock40	1	Point-to-point	LVDS	40.08Mhz
Fast Control Bus				
Ccb_clock40_enable	1	Bussed	GTLP	Pulse, (n) counts
Ccb_cmd[5..0]	6	Bussed	GTLP	Level
Ccb_evcntres	1	Bussed	GTLP	25 ns
Ccb_bcntres	1	Bussed	GTLP	25 ns
Ccb_cmd_strobe	1	Bussed	GTLP	25 ns
Ccb_bc0	1	Bussed	GTLP	25 ns
Ccb_l1accept	1	Bussed	GTLP	25 ns
Ccb_data[7..0]	8	Bussed	GTLP	Level
Ccb_data_strobe	1	Bussed	GTLP	25 ns
Ccb_ttcrx_ready	1	Bussed	GTLP	Level
Ccb_reserved[4..1]	4	Bussed	GTLP	25 ns
Total	26			
MPC Reload Bus				
Mpc_hard_reset	1	Point-to-point	GTLP	300 ns
Mpc_cfg_done	1	Point-to-point	GTLP	Level
Mpc_soft_reset (former Mpc_reserved[2])	1	Point-to-point	GTLP	25 ns
Mpc_reserved[1..0]	2	Point-to-point	GTLP	25 ns
Total	5			

Table 2

Commands decoded from the ccb_cmd[5..0] lines

Command	Ccb_cmd[5..0] code (hex)	Comment
BC0	1	Bunch crossing counter BXN[1..0] starts counting on next clock tick
L1Reset	3	Load initial value into BXN[1..0] counter, generates 3.2 us negative pulse on TX_EN pin of TLK2501 transmitters (IDLE mode)
Inject patterns from MPC	30	Send test patterns from the MPC FIFO_A to SP

2. Interface to Trigger Motherboard

The TMB sends two LCTs to MPC every 25 ns. Each LCT comprises 32 bits that are sent in two frames at 80 Mhz. Preliminary frame format is shown in Table 3.

The MPC sorting logic accepts 18 4-bit patterns "Quality[3..0]" that represent the "quality" of each incoming LCT and outputs three 18-bit binary addresses of the first, second and third largest patterns. These 54 bits are used for the LCT merging onto sorter outputs. Selected 32-bit patterns are multiplexed in two 16-bit frames on the FPGA outputs and sent directly to TLK2501 serializers [6] in ranked order (see Section 3).

The MPC chooses the best three out of 18 patterns it receives every 25 ns clock cycle. If a particular pattern is accepted by the MPC, a "winner" bit is sent from MPC to corresponding TMB. The total number of "winner" bits is 18, and they are sent back to TMB's in two 80Mhz frames. Each TMB will insert two corresponding bits into one of its streams to DMB for further monitoring. The "1" in the first frame indicates that an LCT0 from the particular TMB was accepted by the MPC. The "1" in the second frame indicates that the LCT1 from the particular TMB was accepted by the MPC.

The MPC compares the lowest bit of the its 2-bit BXN counter against bit BXN[0] of each LCT arriving from the TMB. The offset of BXN counter can be preprogrammed using CSR0[3:2] bits. SyEr bit which is sent to SP (and FIFO_B) per each muon is an OR of the comparator output and corresponding SyEr bit from the particular "winning" TMB. Comparator outputs can be masked with the MASKCOMP bit of CSR0 and SyEr bits from "winning" TMBs can be masked with the MASKTMB bit of CSR0. If mask=0, then the source is enabled. Both mask bits can be useful for board debugging, testing and searching for the source of possible synchronization errors.

Table 3

TMB-to-MPC data Format

First frame transmitted at 80MHz			Second frame transmitted at 80Mhz		
Bit	Signal	LCT	Bit	Signal	LCT
0	Wire Group_0	0	0	½-strip_0	0
1	Wire Group_1	0	1	½-strip_1	0
2	Wire Group_2	0	2	½-strip_2	0
3	Wire Group_3	0	3	½-strip_3	0
4	Wire Group_4	0	4	½-strip_4	0
5	Wire Group_5	0	5	½-strip_5	0
6	Wire Group_6	0	6	½-strip_6	0
7	CLCT Pattern_ID0	0	7	½-strip_7	0
8	CLCT Pattern_ID1	0	8	L/R Bend Angle	0
9	CLCT Pattern_ID2	0	9	SYNC_ER	0
10	CLCT Pattern_ID3	0	10	BXN[0]	0
11	**Quality_0 (used for sorting)**	0	11	BC0	0
12	**Quality_1 (used for sorting)**	0	12	CSC_ID0	0
13	**Quality_2 (used for sorting)**	0	13	CSC_ID1	0
14	**Quality_3 (used for sorting)**	0	14	CSC_ID2	0
15	Valid Pattern Flag	0	15	CSC_ID3	0
16	Wire Group_0	1	16	½-strip_0	1
17	Wire Group_1	1	17	½-strip_1	1
18	Wire Group_2	1	18	½-strip_2	1
19	Wire Group_3	1	19	½-strip_3	1
20	Wire Group_4	1	20	½-strip_4	1
21	Wire Group_5	1	21	½-strip_5	1
22	Wire Group_6	1	22	½-strip_6	1
23	CLCT Pattern_ID0	1	23	½-strip_7	1
24	CLCT Pattern_ID1	1	24	L/R Bend Angle	1
25	CLCT Pattern_ID2	1	25	SYNC_ER	1
26	CLCT Pattern_ID3	1	26	BXN[0]	1
27	**Quality_0 (used for sorting)**	1	27	BC0	1
28	**Quality_1 (used for sorting)**	1	28	CSC_ID0	1
29	**Quality_2 (used for sorting)**	1	29	CSC_ID1	1
30	**Quality_3 (used for sorting)**	1	30	CSC_ID2	1
31	Valid Pattern Flag	1	31	CSC_ID3	1

All signals from nine TMB's (32*9=288 lines) to MPC as well as nine "winner" bits are point-to-point lines and transmitted using "negative" (active "0") GTLP logic. They are terminated (56 Ohm to +1.5V) on the MPC board. Pin assignment for all four backplane connectors at the MPC slot 12 is given in Tables 4..7 (connector numbers are referred to [7]). Two sources of +1.5V power (Tables 6-7) can be used for GTLP termination. There is also a possibility to obtain +1.5V from an on-board voltage regulator.

Table 4

Pin assignment of the X36 backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	CLK+	B1	CLK-	C1	GND	D1	Mpc_hreset	E1	Mpc_rsv0
A2		B2		C2	GND	D2	Mpc_rsv1	E2	Mpc_rsv2
A3		B3		C3	GND	D3		E3	Mpc_cfg_d
A4		B4		C4	GND	D4		E4	
A5	Clk_enable	B5	Ccb_rsv4	C5	GND	D5		E5	
A6	Ccm_cmd0	B6	Ccb_cmd1	C6	GND	D6	Ccb_cmd2	E6	Ccb_cmd3
A7	Ccb_cmd4	B7	Ccb_cmd5	C7	GND	D7	Ccb_evcnres	E7	Ccb_bcntres
A8	Ccb_cmd_str	B8	Ccb_bx0	C8	GND	D8	Ccb_l1a	E8	Ccb_dstrobe
A9	Ccb_data0	B9	Ccb_data1	C9	GND	D9	Ccb_data2	E9	Ccb_data3
A10	Ccb_data4	B10	Ccb_data5	C10	GND	D10	Ccb_data6	E10	Ccb_data7
A11	Ccb_ttcrx_rd	B11	Ccb_rsv1	C11	GND	D11	Ccb_rsv2	E11	Ccb_rsv3
A12	Lct8_vpf	B12	Lct8_qual0	C12	GND	D12	Lct8_qual1	E12	Lct8_qual2
A13	Lct8_qual3	B13	Lct8_qual4	C13	GND	D13	Lct8_qual5	E13	Lct8_qual6
A14	Lct8_qual7	B14	Lct8_qual8	C14	GND	D14	Lct8_hs0	E14	Lct8_hs1
A15	Lct8_hs2	B15	Lct8_hs3	C15	GND	D15	Lct8_hs4	E15	Lct8_hs5
A16	Lct8_hs6	B16	Lct8_hs7	C16	GND	D16	Lct8_wg0	E16	Lct8_wg1
A17	Lct8_wg2	B17	Lct8_wg3	C17	GND	D17	Lct8_wg4	E17	Lct_wg5
A18	Lct8_wg6	B18	Lct8_accmu	C18	GND	D18	Lct8_bxn0	E18	Lct8_bc0
A19	Lct8_rsv0	B19	Lct8_rsv1	C19	GND	D19	Lct8_rsv2	E19	Lct8_rsv3
A20	Lct2_vpf	B20	Lct2_qual0	C20	GND	D20	Lct2_qual1	E20	Lct2_qual2
A21	Lct2_qual3	B21	Lct2_qual4	C21	GND	D21	Lct2_qual5	E21	Lct2_qual6
A22	Lct2_qual7	B22	Lct2_qual8	C22	GND	D22	Lct2_hs0	E22	Lct2_hs1
A23	Lct2_hs2	B23	Lct2_hs3	C23	GND	D23	Lct2_hs4	E23	Lct2_hs5
A24	Lct2_hs6	B24	Lct2_hs7	C24	GND	D24	Lct2_wg0	E24	Lct2_wg1
A25	Lct2_wg2	B25	Lct2_wg3	C25	GND	D25	Lct2_wg4	E25	Lct2_wg5

Table 5

Pin assignment of the X37 backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Lct2_wg6	B1	Lct2_accmu	C1	GND	D1	Lct2_bxn0	E1	Lct2_bc0
A2	Lct2_rsv0	B2	Lct2_rsv1	C2	GND	D2	Lct2_rsv2	E2	Lct2_rsv3
A3	Lct2_winner	B3	Lct4_winner	C3	GND	D3	Lct6_winner	E3	Lct8_winner
A4	Lct6_vpf	B4	Lct6_qual0	C4	GND	D4	Lct6_qual1	E4	Lct6_qual2
A5	Lct6_qual3	B5	Lct6_qual4	C5	GND	D5	Lct6_qual5	E5	Lct6_qual6
A6	Lct6_qual7	B6	Lct6_qual8	C6	GND	D6	Lct6_hs0	E6	Lct6_hs1
A7	Lct6_hs2	B7	Lct6_hs3	C7	GND	D7	Lct6_hs4	E7	Lct6_hs5
A8	Lct6_hs6	B8	Lct6_hs7	C8	GND	D8	Lct6_wg0	E8	Lct6_wg1
A9	Lct6_wg2	B9	Lct6_wg3	C9	GND	D9	Lct6_wg4	E9	Lct6_wg5
A10	Lct6_wg6	B10	Lct6_accmu	C10	GND	D10	Lct6_bxn0	E10	Lct6_bc0
A11	Lct6_rsv0	B11	Lct6_rsv1	C11	GND	D11	Lct6_rsv2	E11	Lct6_rsv3

Table 6

Pin assignment of the X38 backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Lct4_vpf	B1	Lct4_qual0	C1	GND	D1	Lct4_qual1	E1	Lct4_qual2

A2	Lct4_qual3	B2	Lct4_qual4	C2	+1.5_1	D2	Lct4_qual5	E2	Lct4_qual6
A3	Lct4_qual7	B3	Lct4_qual8	C3	GND	D3	Lct4_hs0	E3	Lct4_hs1
A4	Lct4_hs2	B4	Lct4_hs3	C4	+1.5_1	D4	Lct4_hs4	E4	Lct4_hs5
A5	Lct4_hs6	B5	Lct4_hs7	C5	GND	D5	Lct4_wg0	E5	Lct4_wg1
A6	Lct4_wg2	B6	Lct4_wg3	C6	+1.5_1	D6	Lct4_wg4	E6	Lct4_wg5
A7	Lct4_wg6	B7	Lct4_accmu	C7	GND	D7	Lct4_bxn0	E7	Lct4_bc0
A8	Lct4_rsv0	B8	Lct4_rsv1	C8	+1.5_1	D8	Lct4_rsv2	E8	Lct4_rsv3
A9	Lct5_vpf	B9	Lct5_qual0	C9	GND	D9	Lct5_qual1	E9	Lct5_qual2
A10	Lct5_qual3	B10	Lct5_qual4	C10	+1.5_1	D10	Lct5_qual5	E10	Lct5_qual6
A11	Lct5_qual7	B11	Lct5_qual8	C11	GND	D11	Lct5_hs0	E11	Lct5_hs1
A12	Lct5_hs2	B12	Lct5_hs3	C12	+1.5_1	D12	Lct5_hs4	E12	Lct5_hs5
A13	Lct5_hs6	B13	Lct5_hs7	C13	GND	D13	Lct5_wg0	E13	Lct5_wg1
A14	Lct5_wg2	B14	Lct5_wg3	C14	+1.5_1	D14	Lct5_wg4	E14	Lct5_wg5
A15	Lct5_wg6	B15	Lct5_accmu	C15	GND	D15	Lct5_bxn0	E15	Lct5_bc0
A16	Lct5_rsv0	B16	Lct5_rsv1	C16	+1.5_1	D16	Lct5_rsv2	E16	Lct5_rsv3
A17	Lct3_vpf	B17	Lct3_qual0	C17	GND	D17	Lct3_qual1	E17	Lct3_qual2
A18	Lct3_qual3	B18	Lct3_qual4	C18	+1.5_1	D18	Lct3_qual5	E18	Lct3_qual6
A19	Lct3_qual7	B19	Lct3_qual8	C19	GND	D19	Lct3_hs0	E19	Lct3_hs1
A20	Lct3_hs2	B20	Lct3_hs3	C20	+1.5_1	D20	Lct3_hs4	E20	Lct3_hs5
A21	Lct3_hs6	B21	Lct3_hs7	C21	GND	D21	Lct3_wg0	E21	Lct3_wg1
A22	Lct3_wg2	B22	Lct3_wg3	C22	+1.5_1	D22	Lct3_wg4	E22	Lct3_wg5
A23	Lct3_wg6	B23	Lct3_accmu	C23	GND	D23	Lct3_bxn0	E23	Lct3_bc0
A24	Lct3_rsv0	B24	Lct3_rsv1	C24	+1.5_1	D24	Lct3_rsv2	E24	Lct3_rsv3
A25	Lct1_winner	B25	Lct3_winner	C25	GND	D25	Lct5_winner	E25	Lct7_winner

Table 7

Pin assignment of the X39 backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Lct7_vpf	B1	Lct7_qual0	C1	GND	D1	Lct7_qual1	E1	Lct7_qual2
A2	Lct7_qual3	B2	Lct7_qual4	C2	+1.5_2	D2	Lct7_qual5	E2	Lct7_qual6
A3	Lct7_qual7	B3	Lct7_qual8	C3	GND	D3	Lct7_hs0	E3	Lct7_hs1
A4	Lct7_hs2	B4	Lct7_hs3	C4	+1.5_2	D4	Lct7_hs4	E4	Lct7_hs5
A5	Lct7_hs6	B5	Lct7_hs7	C5	GND	D5	Lct7_wg0	E5	Lct7_wg1
A6	Lct7_wg2	B6	Lct7_wg3	C6	+1.5_2	D6	Lct7_wg4	E6	Lct7_wg5
A7	Lct7_wg6	B7	Lct7_accmu	C7	GND	D7	Lct7_bxn0	E7	Lct7_bc0
A8	Lct7_rsv0	B8	Lct7_rsv1	C8	+1.5_2	D8	Lct7_rsv2	E8	Lct7_rsv3
A9	Lct1_vpf	B9	Lct1_qual0	C9	GND	D9	Lct1_qual1	E9	Lct1_qual2
A10	Lct1_qual3	B10	Lct1_qual4	C10	+1.5_2	D10	Lct1_qual5	E10	Lct1_qual6
A11	Lct1_qual7	B11	Lct1_qual8	C11	GND	D11	Lct1_hs0	E11	Lct1_hs1
A12	Lct1_hs2	B12	Lct1_hs3	C12	+1.5_2	D12	Lct1_hs4	E12	Lct1_hs5
A13	Lct1_hs6	B13	Lct1_hs7	C13	GND	D13	Lct1_wg0	E13	Lct1_wg1
A14	Lct1_wg2	B14	Lct1_wg3	C14	+1.5_2	D14	Lct1_wg4	E14	Lct1_wg5
A15	Lct1_wg6	B15	Lct1_accmu	C15	GND	D15	Lct1_bxn0	E15	Lct1_bc0
A16	Lct1_rsv0	B16	Lct1_rsv1	C16	+1.5_2	D16	Lct1_rsv2	E16	Lct1_rsv3
A17	Lct9_vpf	B17	Lct9_qual0	C17	GND	D17	Lct9_qual1	E17	Lct9_qual2
A18	Lct9_qual3	B18	Lct9_qual4	C18	+1.5_2	D18	Lct9_qual5	E18	Lct9_qual6
A19	Lct9_qual7	B19	Lct9_qual8	C19	GND	D19	Lct9_hs0	E19	Lct9_hs1
A20	Lct9_hs2	B20	Lct9_hs3	C20	+1.5_2	D20	Lct9_hs4	E20	Lct9_hs5
A21	Lct9_hs6	B21	Lct9_hs7	C21	GND	D21	Lct9_wg0	E21	Lct9_wg1
A22	Lct9_wg2	B22	Lct9_wg3	C22	+1.5_2	D22	Lct9_wg4	E22	Lct9_wg5
A23	Lct9_wg6	B23	Lct9_accmu	C23	GND	D23	Lct9_bxn0	E23	Lct9_bc0
A24	Lct9_rsv0	B24	Lct9_rsv1	C24	+1.5_2	D24	Lct9_rsv2	E24	Lct9_rsv3
A25	Lct9_winner	B25		C25	GND	D25		E25	

3. Interface to Sector Processor

Three best patterns (or two in case of Station 1) selected by sorting logic are sent at 80Mhz from the processing FPGA to three 16-bit TLK2501 serializers, one pattern per one serializer. They perform a parallel-to-serial data conversion with 8B/10B decoding. A serialized data is sent to Finisar FTRJ-8519-1-2.5 [8] small form factor (SFF) optical transmitters and further over 100 m optical cables to SP.

The TLK2501 serializer performs both serial-to-parallel and parallel-to-serial data conversion. The transmitter latches 16-bit parallel data at a reference clock rate and internally encodes it using 8B/10B format. The resulting 20-bit word is transmitted differentially at 20 times the reference clock frequency. The receiver section on a SP board performs a serial-to-parallel conversion on the input data, synchronizes the resulting 20-bit wide parallel word to the extracted reference clock and applies the 8B/10B decoding. The 80Mhz to 125Mhz frequency range for the reference clock allows us to transfer data at 80.16Mhz which is exactly double the LHC operating frequency of 40.08Mhz. The device has a built-in 8-bit pseudo-random bit stream generator and some other useful features such as a loss of signal detection circuit and power down mode. The device is powered from +2.5V and consumes less than 325mW. Parallel data, control and status pins are 3.3V compatible.

Finisar FTRJ-8519-1-2.5 2x5 pinned SFF transceivers provides bidirectional communication at data rates up to 2.125Gbps (1.6Gbps simplex mode transmission is required in our case). The laser technology is an 850 nm multimode VCSEL. It allows fiber lengths up to 300 m. The transceiver operates at extended voltages (3.15V to 3.60V) and temperature (-10C to +85C) ranges and dissipates less than 750mW. One advantage of the FTRJ-8519-1-2.5 module over similar optical transceivers available from other vendors is a metal enclosure for lower electromagnetic interference.

As described above, each selected by MPC pattern comprises 32 bit. It is transmitted to SP in two 16-bit frames at 80Mhz. The frame format is shown in Table 8.

Table 8

MPC-to-SP Data Format

Frame 1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vpf	**Quality[3..0]**				**CLCT Pattern ID[3..0]**				**Wire Group ID[6..0]**						
Frame 2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip Pattern_ID[7..0]**							

CLCT Half-Strip Pattern ID is between 0 and 159
CLCT Pattern encodes the number of layers and whether the pattern consists of half-strips or di-strips
Wire Group ID is between 0 and 111 and indicates the position of the pattern within the chamber
L/R – Bend Angle Bit indicates whether the track is heading towards lower or higher strip number
VPF – Valid Pattern Flag indicates a valid LCT that has been found by TMB and being sent in the current clock cycle
ER - Synchronization Error
BX0 – The less significant bits of Bunch Crossing Counter
BC0 – Bunch Crossing Zero Flag arriving from the TMB

4. VME Interface

The MPC recognizes both geographical and logical (defined by on-board switch) A24D16 addresses. Geographical mode utilizes geographical address lines GA[4..0] available on VME64x backplane. In this mode the MPC recognizes its address space when the code on address lines A[23..19] is equal to 5-bit geographical address of the slot in a crate where it is located. The MPC resides on slot 12 of the peripheral EMU backplane, so its base geographical address is 600000(hex). An MPC recognizes AM codes 39(hex) (non-privileged access) and 3D(hex) (supervisor access). Decoded addresses and VME commands are listed in Table 9. The MPC does not respond to byte-addressing modes, so all valid addresses must be even numbers. Input and Output FIFO buffers and Control and Status Registers (CSR) are described in Sections 7 and 8 respectively.

The main part of the VME interface (data drivers, address latches, address comparators, DTACK response scheme, CSR0) is implemented in a glue logic. This means that the board is accessible even without the mezzanine card that carries a processing FPGA. CSR[1-3] and FIFO buffers are designed inside FPGA, so the board still will be responding to their addresses even in case of absence of the mezzanine card, but data won't be valid.

Table 9

Address (hex)	Access	Function
X00000	Read/Write	CSR0
X00080	Read/Write	FIFO_A1[15..0]. Corresponds to TMB1
X00082	Read/Write	FIFO_A1[31..16]. Corresponds to TMB1
X00084	Read/Write	FIFO_A2[15..0]. Corresponds to TMB2
X00086	Read/Write	FIFO_A2[31..16]. Corresponds to TMB2
X00088	Read/Write	FIFO_A3[15..0]. Corresponds to TMB3
X0008A	Read/Write	FIFO_A3[31..16]. Corresponds to TMB3
X0008C	Read/Write	FIFO_A4[15..0]. Corresponds to TMB4
X0008E	Read/Write	FIFO_A4[31..16]. Corresponds to TMB4
X00090	Read/Write	FIFO_A5[15..0]. Corresponds to TMB5
X00092	Read/Write	FIFO_A5[31..16]. Corresponds to TMB5
X00094	Read/Write	FIFO_A6[15..0]. Corresponds to TMB6
X00096	Read/Write	FIFO_A6[31..16]. Corresponds to TMB6
X00098	Read/Write	FIFO_A7[15..0]. Corresponds to TMB7
X0009A	Read/Write	FIFO_A7[31..16]. Corresponds to TMB7
X0009C	Read/Write	FIFO_A8[15..0]. Corresponds to TMB8
X0009E	Read/Write	FIFO_A8[31..16]. Corresponds to TMB8
X000A0	Read/Write	FIFO_A9[15..0]. Corresponds to TMB9
X000A2	Read/Write	FIFO_A9[31..16]. Corresponds to TMB9
X000A4	Read/Write	FIFO_B1[15..0]. Corresponds to 1st best selected LCT
X000A6	Read/Write	FIFO_B2[15..0]. Corresponds to 2nd best selected LCT
X000A8	Read/Write	FIFO_B3[15..0]. Corresponds to 3rd best selected LCT
X000AA	Read/Write	CSR1 (date of the current firmware version)
X000AC	Read/Write	CSR2 (reserved for future use)
X000AE	Read	CSR3 (FIFO Status)
X000B0	Read	L1ACC Counter
X000B2	Write	Transmit 511 words of data from all FIFO_A buffers in "Test" mode
X000B4	Write	

X000B6	Write	Send TxEn "0" pulse to all three TLK2501 transmitters
X000B8		

5. FIFO Buffers

Two groups of FIFO Buffers (FIFO_A and FIFO_B) are implemented in the main FPGA in order to test the MPC internal functionality and its communications with Trigger Motherboards and Sector Processor. Both buffers are 511-word deep and available from VME for read and write (Table 8). Since two muon patterns are packed into FIFO_A in two frames, each FIFO effectively comprises 255 patterns. Each buffer represents data corresponding to one TMB board, or two muon patterns. FIFO_A1 corresponds to TMB1, FIFO_A2 corresponds to TMB2 and so on. Its format is shown in Table 10. In a "Test" mode the test patterns representing 18 muons can be send out simultaneously from all FIFO_A buffers at 80Mhz upon specific VME command. They pass through the sorting logic that selects three best and transmits them to SP and fed into FIFO_B also at 80MHz. FIFO_B format is shown in Table 11. In a "Trigger" mode the selected patterns from TMB's act as a data sources until FIFO_B is full.

One important feature of all FIFO_B buffers is that the data from FIFO_A ("Test" mode) or TMB's ("Trigger" mode) can be saved in FIFO_B only if there is at least one valid muon pattern, or pattern with vpf=1. This allows acquiring into FIFO_B the data, representing only valid patterns. The vpf bit from the first best selected muon acts as a "write enable" signal for all FIFO_B buffers. This means that if there is just one valid pattern coming after sorting from FIFO_A or TMB, it will be stored in FIFO_B1 and "0" will be written into FIFO_B[2..3]. This assures that all three FIFO_B buffers will contain an equal number of words inside. As for VME access, any data can be loaded and read back out of any FIFO_B buffer independently.

FULL and EMPTY flags (common to all FIFO_A and FIFO_B buffers) are available for read from CSR2. After asynchronous FIFO reset all these flags are active "1".

Table 10

FIFO_A Data Format

FIFO_A Frame 1 (LCT0)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
vpf	**Quality[3..0]**				**CLCT Pattern[3..0]**				**Wire Group ID[6..0]**						
FIFO_A Frame 1 (LCT1)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
vpf	**Quality[3..0]**				**CLCT Pattern[3..0]**				**Wire Group ID[6..0]**						
FIFO_A Frame 2 (LCT0)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC_ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip ID[7..0]**							
FIFO_A Frame 2 (LCT1)															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CSC_ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip ID[7..0]**							

Table 11

FIFO_B Data Format

FIFO_B Frame 1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vpf	**Quality[3..0]**				**CLCT Pattern ID[3..0]**				**Wire Group ID[6..0]**						
FIFO_B Frame 2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSC_ID[3..0]				**Bc0**	**Bx0**	**ER**	**L/R**	**CLCT Half-strip Pattern_ID[7..0]**							

6. Control and Status Registers

The 16-bit CSR0 is implemented in glue logic and available for write and read over VME even if the main mezzanine card is not installed. Bit assignment is shown in Table 12. CSR[1-3] are implemented inside FPGA. Their formats are shown in Tables 13-15.

Table 12

CSR0 (glue logic outside FPGA)

Bit and access	Function
0 (R/W)	FPGA_Mode (Trigger mode if "0", Test mode (FIFO_A is a source of data) if "1")
1(R/W)	Reset FPGA logic (FIFO buffers, counters) (Active "1")
2 (R/W)	BXN[0] offset
3 (R/W)	BXN[1] offset
4 (R/W)	FPGA Hard Reset (OR'ed with the Hard Reset from CCB) (Active "0")
5 (R/W)	TDI (JTAG signal for FPGA/EPROM access)
6 (R/W)	TMS (JTAG signal for FPGA/EPROM access)
7 (R/W)	TCK (JTAG signal for FPGA/EPROM access)
8 (R)	TDO (JTAG signal for FPGA/EPROM access)
9 (R/W)	TxEn signal for TLK2501 transmitters
10 (R/W)	MASKTMB (Mask ER bits from each winning TMB or FIFO_A (enabled if "0" and disabled if "1")
11 (R/W)	MASKCOMP (Mask all outputs of BXN comparators (enabled if "0" and disabled if "1")
12 (R)	FPGA Configuration Done (read only, active "1")
13 (R)	"0"
14 (R/W)	Enable TLK2501 serializers. If "0", all TLK2501 are in power-down mode
15 (R/W)	PRBSEN (Enable PRBS test mode for all TLK2501 serializers)

Table 13

CSR1 (inside FPGA, contains the date of the firmware version)

Bit and access	Function
0 (R)	Day, LSB
1(R)	Day
2 (R)	Day
3 (R)	Day
4 (R)	Day, MSB
5 (R)	Month, LSB
6 (R)	Month
7 (R)	Month
8 (R)	Month, MSB

9 (R)	Year, LSB (*)
10 (R)	Year (*)
11 (R)	Year, MSB (*)
12 (R)	“0”
13 (R)	“0”
14 (R)	“0”
15 (R)	“0”

(*) The code at CSR1<11..9> should be added to 2000 to get an actual year. For example, CSR1=1252(dec) corresponds to July 4, 2002.

Table 14

CSR2 (inside FPGA, reserved for future use)

Bit and access	Function
0 (R/W)	When “0”, all TLK2501 transmitters are in “Normal data character” mode. When “1”, all TLK2501 are in IDLE mode, unless there is a Valid Pattern or BC0 from TMB
1(R/W)	
2 (R/W)	
3 (R/W)	
4 (R/W)	
5 (R/W)	
6 (R/W)	
7 (R/W)	
8 (R/W)	
9 (R/W)	
10 (R/W)	
11 (R/W)	
12 (R/W)	
13 (R/W)	
14 (R/W)	
15 (R/W)	

Table 15

CSR3 (inside FPGA)

Bit and access	Function
0 (R)	FIFO_A FULL. Active “1” if at least one out of nine FIFO_A buffers is full
1(R)	FIFO_A EMPTY. Active “1” if ALL nine FIFO_A buffers are empty. Also “1” after reset
2 (R)	FIFO_B FULL. Active “1” if at least one out of three FIFO_B buffers is full
3 (R)	FIFO_B EMPTY. Active “1” if ALL three FIFO_B buffers are empty. Also “1” after reset
4 (R)	“0”
5 (R)	“0”
6 (R)	“0”
7 (R)	“0”
8 (R)	“0”
9 (R)	“0”
10 (R)	“0”
11 (R)	“0”
12 (R)	“0”
13 (R)	“0”
14 (R)	“0”
15 (R)	“0”

7. Mezzanine Board and JTAG Access to FPGA and EPROM

A mezzanine card designed at UCLA will be used. It comprises one Xilinx XCV1000E-7FG680C or pin-compatible XCV600E-7FG680C FPGA and three XC18V04 EPROM which are accessible over JTAG bus. JTAG signals can be emulated using write and read operations directed to bits 5-8 of CSR0. There is no dedicated JTAG controller on the MPC board . In addition to that a JTAG access from external computer is also possible. An on-board jumper defines which of these two options is activated. Two connectors for external JTAG cables may be used. One is compatible with a recommended Xilinx Parallel Cable III [9] and another one is compatible with a UCLA differential JTAG cable [10]. Only one cable can be connected at a time.

Two clock signals for the FPGA are provided from the main MPC board. Either CCB clock obtained from the backplane or an internal 40.08Mhz clock from on-board oscillator (80.16Mhz divided by two) can be used. One of these clocks can be delayed on the main board using 3D7408 delay line from Data Delay Devices. The delay value can be set using on-board jumpers S5.

8. Initialization and Programming

The board initialization includes programming of the CSR0 and sending "Reset" signal to FPGA logic (write "0", then "1", then again "0" into CSR0[1]). In order to check the sorter logic, FIFO_A should be programmed (the last word written into all FIFO_A buffers should be "0") , then write command to address x000b2(hex) should be sent (start transmission from FIFO_A), and finally FIFO_B content should be checked.

9. Fuses

Fuse F10 provides +5V power from VME J1 backplane. Fuse F7 provides +1.8V power for the mezzanine FPGA. Fuse F9 provides +2.5V power for TLK2501 transceivers. All these fuses are required at any time.

Fuse F8 provides +3.3V power from J1 VME64x backplane while fuse F11 provides +3.3V from on-board voltage regulator U65. Only one (either F8 or F11) fuse should be installed at a time. In case of VME64x backplane the F8 is recommended.

Fuses F5 and F6 provide +3.3V power for Xilinx downloading cables, differential and regular (see Section 7). Both should be installed.

Fuses F1-F4 provide reference voltages for GTLP transceivers (+1.0V) and GTLP terminators (+1.5V). Fuses F1 and F3 provide these powers from custom backplane (only one should be installed at a time) while F2 and F4 provide powers from on-board voltage regulator U64 (only one should be installed at a time). It is recommended to use F3 and F1 when custom backplane is being used.

10. Switches

Switch S1 is needed to select the source of the master clock. If S1 1-4 are connected, the source is 40.08 clock from CCB. If S1 2-3 are connected, the source is on-board quartz oscillator (80.16 Mhz divided by 2). The standard option is when S1 1-4 are "on".

Switch S2 provides both master (when S2 1-4 are connected) and delayed master (when S2 2-3 are connected) clocks to the mezzanine FPGA. The delay value can be set by S5 with the minimal step of 0.25 ns. The delayed clock is not used by the current version of the MPC firmware.

Switches S3, S4 and S6 are needed to select the source of the reference 80.16Mhz clock for the TLK2501 transmitters (channels 1, 2 and 3 respectively). When 1-4 are "on" the clock comes from a dedicated clock driver (standard option). When 2-3 are connected, the source is a clock provided by the FPGA using its own DLL (for testing purposes only).

Switch S8 is needed to chose the source of JTAG access to mezzanine FPGA. When S8 1-4 are connected, the source is one of two JTAG cables. When S8 1-4 are disconnected, the source is CSR0[5..8]. S8 2-3 are not used. Switch S7 is used to connect one of two JTAG cables to FPGA when S8 1-4 are "on". If S7 1-16, 3-14, 5-12, 7-10 are "on" and 2-15, 4-13, 6-11, 8-9 are "off", the source is a differential cable (connector P9). If S7 1-16, 3-14, 5-12, 7-10 are "off" and 2-15, 4-13, 6-11, 8-9 are "on", the source is a regular cable (connector P10).

Switches S9 and S10 are used to chose the mode of addressing (logical or geographical) and select the base address value. When S9 6-7 are connected, the highest A[23..19] addresses are compared with the code defined by other S9 positions (see Table 16). When S9 6-7 are disconnected, the highest A[23..19] addresses are compared with GA[4..0] pins. In both cases A[18..16]="0". Switch S10 is used to define the A[15..8] bits of the base address. When any switch is "on", the respective bit is set to "0". When any switch is "off", the respective bit is set to "1".

Table 20

Bit	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8
Switch	S9								S10							
	5-8	4-9	3-10	2-11	1-12	"0"	"0"	"0"	8-9	7-10	6-11	5-12	4-13	3-14	2-15	1-16

11. Front Panel

There are on the front panel:

- Three optical modules for communication with Sector Processor
- Three red LEDs "MUON[1..3] (with one-shots) that indicate "vpf" bits of three output patterns passing to SP and FIFO_B (D1-D3 respectively)

- Green LED “DONE” (D4) indicates that FPGA configuration and initialization done properly and the DLL is locked
- Yellow LED “TEST” (D5) indicates “Test” mode active
- Green LED “TXEN” (D6) indicates that all three TLK2501 serializers are enabled (not in power down mode)
- Red LED “TCK” (D7) indicates access to JTAG from VME (through CSR0)
- Yellow LED “DACK” (D9, with one-shot) indicates an access to MPC over VME
- Green LED “GEOG” (D8) indicates that geographical address mode is selected
- Green LEDs “+5V” (D18), “+3.3V” (D19), “+2.5V” (D20), “+1.8V” (D21), “+1.5VA” (D22) and “+1.5VB” (D23) indicate an active on-board power supplies
- Red LED “IDLE” (D10) indicates that all three TLK2501 serializers are switched into IDLE mode
- Red LED “RNTS” (Run Test) (D11) indicates that data transmission from FIFO_A buffer was initiated upon VME command
- Red LED “L1RS” (L1 Reset) (D12) indicates that L1 Reset command had been decoded by the MPC
- Red LED “FAEM” (FIFO_A Empty) (D13) indicates that all nine FIFO_A buffers are empty
- Red LED “FBEM” (FIFO_B Empty) (D14) indicates that all three FIFO_B buffers are empty
- Red LED “FAFL” (FIFO_A Full) (D15) indicated that at least one out of nine FIFO_A buffers is full
- Red LED “FBFL” (FIFO_B Full) (D16) indicated that at least one out of three FIFO_B buffers is full
- 1 reserved red LED (D17)

References

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History

12/18/2001. TMB-to-MPC and MPC-to-SP data formats (Tables 2 and 7) were changed
01/07/2002. CSR0 format was changed.
02/12/2002. Changes in CSR0 format

05/21/2002: Changes is VME addresses. Changes in CSR0 format.
07/22/2002: Changes in TMB-to-MPC and MPC-to-SP data formats. CSR1 has been specified.
03/28/2003: CSR0[13] was changed.
04/03/2003: Section 1 was expanded. Sections 8 (Fuses) and 9 (Switches) were added.
04/07/2003: Section 8 (Initialization and Programming) was added.
05/28/2003: CSR2[0] was added. An IDLE pulse on TX_EN pin of TLK2501 transmitters was expanded to 3.2 us. Firmware version 05/19/2003, see
http://bonner-ntserver.rice.edu/cms/mpc1b.mcs