The Muon Sorter Board for the Cathode Strip Chamber Trigger Electronics at the CMS Experiment

Specification

Version 2.0

Rice University

05/04/2004

Introduction

The Track Finder (TF) for the Cathode Strip Chamber (CSC) trigger electronics consists of twelve Sector Processors (SP), one Muon Sorter (MS) and Clock and Control Board (CCB). Each SP receives the optical data streams from several Muon Port Cards (MPC) residing in the peripheral CSC crates, measures the transverse momentum, pseudo-rapidity and azimuthal angle of each muon and sends up to 3 selected muons to the MS. The MS selects four best muon candidates out of 36 possible and transmits them to Global Muon Trigger (GMT) receiver module over four copper cables.

The TF crate and GMT/Global Trigger crate are located in the underground counting room. All communication between Sector Processors, Muon Sorter and Clock and Control Board is implemented over custom 6U backplane residing below the 3U VME backplane in the 9U*400 mm crate. The functionality and external connections of the MS are described below. Block diagram of the MS board is shown on Figure 1. It comprises the backplane interface, VME interface, main processing logic based on Xilinx FPGA, located on a mezzanine card, and an LVDS transmitters to GMT crate.

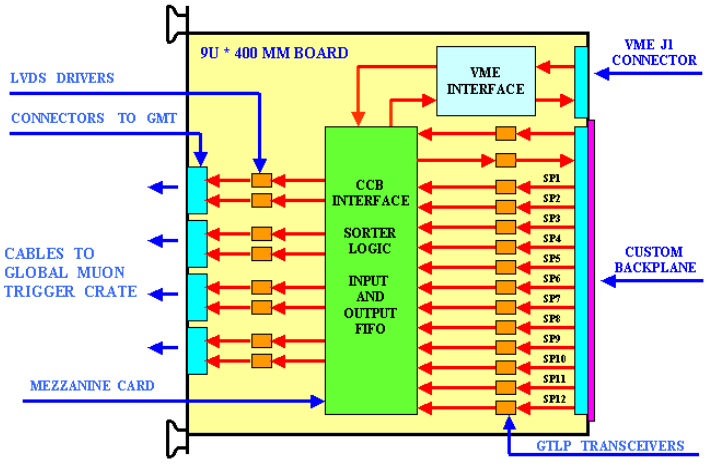

Figure 1: Muon Sorter Board Block Diagram

1. Interface to Clock and Control Board

The CCB distributes several common (bussed) and individual (point-to-point) signals to each module in the Track Finder crate. A full list of these signals is given in [1]. Its subset relevant to MS is shown in Table 1. While the 40.08Mhz clock signal from CCB is distributed over LVDS lines individually to each board in a crate, the other signals are transmitted using GTLP logic standard, with active level "0".

The MS may generate the MS_L1A_Request signal to CCB when there is at least one valid muon after the sorting. Generation of this signal can be enabled and disabled using CSR0<7>. There are four reserved signals from the CCB to MS and two reserved signals from the MS to CCB.

The list of commands being decoded from the ccb_cmd[5..0] lines is shown in Table 2.

Table 1: CCB-to-MS Signals

Signal	Bits	Type	Logic	Duration
Clock Bus				
Ccb_clock40	1	Point-to-point, input	LVDS	40.08Mhz
Fast Control Bus				
Ccb_clock40_enable	1	Bussed, input	GTLP	Pulse, (n) counts
Ccb_cmd[5..0]	6	Bussed, input	GTLP	Level
Ccb_evcntres	1	Bussed, input	GTLP	25 ns
Ccb_bcntres	1	Bussed, input	GTLP	25 ns
Ccb_cmd_strobe	1	Bussed, input	GTLP	25 ns
Ccb_bc0	1	Bussed, input	GTLP	25 ns
Ccb_l1accept	1	Bussed, input	GTLP	25 ns
Ccb_data[7..0]	8	Bussed, input	GTLP	Level
Ccb_data_strobe	1	Bussed, input	GTLP	25 ns
Ccb_ttcrx_ready	1	Bussed, input	GTLP	Level
Ccb_reserved[4..1]	4	Bussed, input	GTLP	25 ns
Reload, Trigger and Reserved Lines				
MS_hard_reset	1	Point-to-point, input	GTLP	300 ns
MS_cfg_done	1	Point-to-point, output	GTLP	Level
MS_L1A_Request	1	Point-to-point, output	GTLP	25 ns
CCB_to_MS[3..0] (reserved)	4	Point-to-point, input	GTLP	
MS_to_CCB[1..0] (reserved)	2	Point-to-point, output	GTLP	

Table 2: Commands decoded from the ccb_cmd[5..0] lines

Command	Ccb_cmd[5..0] code (hex)	Comment
BC0	1	Bunch crossing counter BXN[3..0] starts counting on the next clock tick
L1Reset	3	Load initial value into BXN[3..0] counter
Hard Reser	4	Reload FPGA from EPROMs
MS_Hard _Reset	11	Reload FPGA from EPROMs
Inject patterns from MS	31	Send test patterns from the FIFO_A to sorter

Two Digital Clock Managers (DCM, see [2]) inside the main Xilinx Virtex-2 FPGA are being used. The DCM1 allows to precisely adjust the phase of input clock in respect to data arriving from SP's. The DCM2 allows to precisely adjust the phase of output clock

in respect to data being send to GMT. Phase adjustment range is +/-128 bits. One bit corresponds to 1/256 of the 40Mhz clock cycle. Phase adjustment can be done dynamically over VME. To increase (decrease) phase by 1 bit, "1" ("0") should be written into the fine phase adjustment registers (Table 13). DCM status bits are available for read over VME from the DCM status register (Table 13).

2. Sorting Logic and Interface to Sector Processors

Each SP sends to MS up to three muons every 25 ns. Each pattern comprises 32 bits that are sent in two frames at 80 Mhz. The frame format based on [3] is shown in Table 3.

The MS sorter accepts 36 7-bit patterns "Rank[6..0]" that represent the "quality" of each incoming pattern and outputs four 36-bit binary addresses of the first, second, third and fourth largest patterns. These 144 bits are used for pattern merging onto the sorter outputs. Some bits of the selected patterns are undergo further LUT conversion (see Section 3) before they are transmitted to GMT. If several selected patterns appear to have the same rank, then the pattern from the source with a largest physical address will be chosen as a 1st best, the pattern from the source with the second largest physical address will be chosen as a 2nd best and so on. Physical addresses SP_ID[3..0] from 1 to 12 are assigned to each Sector Processor in the MS firmware. It is assumed that if there are no valid muons selected by the Sector Processor, then each SP sends a Rank[6..0]=0.

If a particular pattern from SP has been accepted by the MS, then a "winner" bit is sent from the MS back to corresponding SP. The total number of feedback "winner" lines is 24, or 2 lines per each SP. The "winner" bits are sent in two 80Mhz frames, encoded as shown in Tables 4 and 5. Each SP may insert its "winner" bits into data stream to DDU for further monitoring. The "winner" bits may be delayed within FPGA for a programmable number of bunch crossings (1..15), defined by CSR0[15..12].

Table 3: SP-to-MS Data Format

First frame transmitted at 80MHz			**Second frame transmitted at 80Mhz**		
Bit	Signal	Muon	Bit	Signal	Muon
0	Phi_0	1	0	Rank_0	1
1	Phi_1	1	1	Rank_1	1
2	Phi_2	1	2	Rank_2	1
3	Phi_3	1	3	Rank_3	1
4	Phi_4	1	4	Rank_4	1
5	Eta_0	1	5	Rank_5	1
6	Eta_1	1	6	Rank_6	1
7	Eta_2	1	7	VC	1
8	Eta_3	1	8	C	1
9	Eta_4	1	9	HL	1
10	Phi_0	2	10	Rank_0	2
11	Phi_1	2	11	Rank_1	2
12	Phi_2	2	12	Rank_2	2
13	Phi_3	2	13	Rank_3	2
14	Phi_4	2	14	Rank_4	2
15	Eta_0	2	15	Rank_5	2
16	Eta_1	2	16	Rank_6	2
17	Eta_2	2	17	VC	2

18	Eta_3	2	18	C	2
19	Eta_4	2	19	HL	2
20	Phi_0	3	20	Rank_0	3
21	Phi_1	3	21	Rank_1	3
22	Phi_2	3	22	Rank_2	3
23	Phi_3	3	23	Rank_3	3
24	Phi_4	3	24	Rank_4	3
25	Eta_0	3	25	Rank_5	3
26	Eta_1	3	26	Rank_6	3
27	Eta_2	3	27	VC	3
28	Eta_3	3	28	C	3
29	Eta_4	3	29	HL	3
30	BC0	Common to 1-3	30	BX0	Common to 1-3
31	SE	Common to 1-3	31	SP	Common to 1-3

VC – Valid Charge (8^{th} bit of Pt LUT output)
C – Charge or Muon Sign
Rank – Pt LUT Output
HL – Halo Muon Trigger
BC0 – Bunch Crossing Zero Flag
Eta – Pseudorapidity
SE – Synchronization Error (Data out of sync)
Phi – Azimuth Coordinate
BX0 – Least significant bit of the bunch crossing counter
SP – Spare bit

Table 4: MS-to-SP "Winner" Bit Data Format (i=1..12)

Line and frame	Function
Wi_0_Frame1	"1" if Muon_1 was selected by MS from SPi
Wi_0_Frame2	"1" if Muon_3 was selected by MS from SPi
Wi_1_Frame1	"1" if Muon_2 was selected by MS from SPi
Wi_1_Frame2	"0"

Table 5: "Winner" Bit Decoding Scheme

Selected Muons from SPi			Winner Bits			
Muon_3	Muon_2	Muon_1	Wi_1_Frame1	Wi_0_Frame1	Wi_1_Frame2	Wi_0_Frame2
-	-	-	0	0	0	0
-	-	+	0	1	0	0
-	+	-	1	0	0	0
-	+	+	1	1	0	0
+	-	-	0	0	0	1
+	-	+	0	1	0	1
+	+	-	1	0	0	1
+	+	+	1	1	0	1

The MS maintains a 4-bit bunch crossing counter BXN. This counter is set to a predefined state (programmed in BXNOFFSET[3..0] bits in CSR0) upon "Bunch Crossing Reset" command from the Trigger, Timing and Control (TTC) System of the experiment and starts counting on the next clock tick after the "Bunch Crossing Zero" command from the TTC. The BX0 bit arriving with selected muon is compared against the least significant bit of this counter. In case of a mismatch the SyncEr bit is generated and transmitted to corresponding GMT link and FIFO_B if MASKCOMP bit of the CSR0 is "1". Another CSR0 bit, called MASKSP, when "1", enables propagation of

SyncEr bits from selected muons to GMT and FIFO_B. When both MASKCOMP and MASKSP are “0”, the SyncEr bits being transmitted to GMT and FIFO_B are all “0”.

All signals from the SP’s (32*12=384 lines) to the MS as well as 24 “winner” lines from the MS to the SP are transmitted over backplane using “negative” (active “0”) GTLP logic. They are terminated (56 Ohm to +1.5V) on the receiver ends. Pin assignment for backplane connectors at the MS slot based on [4] is given in Tables 6..9.

Table 6: Pin assignment of the X23 [4] backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	CLK+	B1	CLK-	C1	Ccb_ttc_rdy	D1	Ccb_rsv1	E1	Ms_hr
A2	Clk_enable	B2	Ccb_rsv4	C2	GND	D2	Ccb_rsv2	E2	Ccb_rsv3
A3	Ccm_cmd0	B3	Ccb_cmd1	C3	GND	D3	Ccb_cmd2	E3	Ccb_cmd3
A4	Ccb_cmd4	B4	Ccb_cmd5	C4	GND	D4	Ccb_evcnres	E4	Ccb_bcntres
A5	Ccb_cmd_str	B5	Ccb_bx0	C5	GND	D5	Ccb_l1a	E5	Ccb_dstrobe
A6	Ccb_data0	B6	Ccb_data1	C6	GND	D6	Ccb_data2	E6	Ccb_data3
A7	Ccb_data4	B7	Ccb_data5	C7	GND	D7	Ccb_data6	E7	Ccb_data7
A8	Ccb_to_ms0	B8	Ccb_to_ms2	C8	GND	D8	Ccb_to_ms2	E8	Ccb_to_ms3
A9	Sp1_2	B9	Sp1_3	C9	GND	D9	Sp1_0	E9	Sp1_1
A10	Sp1_6	B10	Sp1_7	C10	GND	D10	Sp1_4	E10	Sp1_5
A11	Sp1_10	B11	Sp1_11	C11	GND	D11	Sp1_8	E11	Sp1_9
A12	Sp1_31	B12	Sp1_14	C12	Sp1_15	D12	Sp1_12	E12	Sp1_13
A13	Sp1_18	B13	Sp1_19	C13	Sp1_20	D13	Sp1_16	E13	Sp1_17
A14	Sp1_23	B14	Sp1_24	C14	Sp1_25	D14	Sp1_21	E14	Sp1_22
A15	Sp1_28	B15	Sp1_29	C15	Sp1_30	D15	Sp1_26	E15	Sp1_27
A16	Sp12_2	B16	Sp12_3	C16	+1.5V	D16	Sp12_0	E16	Sp12_1
A17	Sp12_6	B17	Sp12_7	C17	+1.5V	D17	Sp12_4	E17	Sp12_5
A18	Sp12_10	B18	Sp12_11	C18	+1.5V	D18	Sp12_8	E18	Sp12_9
A19	Sp12_14	B19	Sp12_15	C19	Sp12_12	D19	Sp12_13	E19	Sp12_31
A20	Sp12_19	B20	Sp12_20	C20	Sp12_16	D20	Sp12_17	E20	Sp12_18
A21	Sp12_24	B21	Sp12_25	C21	Sp12_21	D21	Sp12_22	E21	Sp12_23
A22	Sp12_29	B22	Sp12_30	C22	Sp12_26	D22	Sp12_27	E22	Sp12_28
A23	Sp3_2	B23	Sp3_3	C23	GND	D23	Sp3_0	E23	Sp3_1
A24	Sp3_6	B24	Sp3_7	C24	GND	D24	Sp3_4	E24	Sp3_5
A25	Sp3_10	B25	Sp3_11	C25	GND	D25	Sp3_8	E25	Sp3_9

Table 7: Pin assignment of the X24 [4] backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Sp3_31	B1	Sp3_14	C1	Sp3_15	D1	Sp3_12	E1	Sp3_13
A2	Sp3_18	B2	Sp3_19	C2	Sp3_20	D2	Sp3_16	E2	Sp3_17
A3	Sp3_23	B3	Sp3_24	C3	Sp3_25	D3	Sp3_21	E3	Sp3_22
A4	Sp3_28	B4	Sp3_29	C4	Sp3_30	D4	Sp3_26	E4	Sp3_27
A5	Sp10_2	B5	Sp10_3	C5	+1.5V	D5	Sp10_0	E5	Sp10_1
A6	Sp10_6	B6	Sp10_7	C6	+1.5V	D6	Sp10_4	E6	Sp10_5
A7	Sp10_10	B7	Sp10_11	C7	+1.5V	D7	Sp10_8	E7	Sp10_9
A8	Sp10_14	B8	Sp10_15	C8	Sp10_12	D8	Sp10_13	E8	Sp10_31
A9	Sp10_19	B9	Sp10_20	C9	Sp10_16	D9	Sp10_17	E9	Sp10_18
A10	Sp10_24	B10	Sp10_25	C10	Sp10_21	D10	Sp10_22	E10	Sp10_23
A11	Sp10_29	B11	Sp10_30	C11	Sp10_26	D11	Sp10_27	E11	Sp10_28
A12	Sp5_2	B12	Sp5_3	C12	GND	D12	Sp5_0	E12	Sp5_1
A13	Sp5_6	B13	Sp5_7	C13	GND	D13	Sp5_4	E13	Sp5_5
A14	Sp5_10	B14	Sp5_11	C14	GND	D14	Sp5_8	E14	Sp5_9
A15	Sp5_31	B15	Sp5_14	C15	Sp5_15	D15	Sp5_12	E15	Sp5_13
A16	Sp5_18	B16	Sp5_19	C16	Sp5_20	D16	Sp5_16	E16	Sp5_17
A17	Sp5_23	B17	Sp5_24	C17	Sp5_25	D17	Sp5_21	E17	Sp5_22
A18	Sp5_28	B18	Sp5_29	C18	Sp5_30	D18	Sp5_26	E18	Sp5_27

A19	Sp8_2	B19	Sp8_3	C19	+1.5V	D19	Sp8_0	E19	Sp8_1
A20	Sp8_6	B20	Sp8_7	C20	+1.5V	D20	Sp8_4	E20	Sp8_5
A21	Sp8_10	B21	Sp8_11	C21	+1.5V	D21	Sp8_8	E21	Sp8_9
A22	Sp8_14	B22	Sp8_15	C22	Sp8_12	D22	Sp8_13	E22	Sp8_31
A23	Sp8_19	B23	Sp8_20	C23	Sp8_16	D23	Sp8_17	E23	Sp8_18
A24	Sp8_24	B24	Sp8_25	C24	Sp8_21	D24	Sp8_22	E24	Sp8_23
A25	Sp8_29	B25	Sp8_30	C25	Sp8_26	D25	Sp8_27	E25	Sp8_28

Table 8: Pin assignment of the X25 [4] backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Sp6_2	B1	Sp6_3	C1	GND	D1	Sp6_0	E1	Sp6_1
A2	Sp6_6	B2	Sp6_7	C2	GND	D2	Sp6_4	E2	Sp6_5
A3	Sp6_10	B3	Sp6_11	C3	GND	D3	Sp6_8	E3	Sp6_9
A4	Sp6_31	B4	Sp6_14	C4	Sp6_15	D4	Sp6_12	E4	Sp6_13
A5	Sp6_18	B5	Sp6_19	C5	Sp6_20	D5	Sp6_16	E5	Sp6_17
A6	Sp6_23	B6	Sp6_24	C6	Sp6_25	D6	Sp6_21	E6	Sp6_22
A7	Sp6_28	B7	Sp6_29	C7	Sp6_30	D7	Sp6_26	E7	Sp6_27
A8	Sp7_2	B8	Sp7_3	C8	+1.5V_1	D8	Sp7_0	E8	Sp7_1
A9	Sp7_6	B9	Sp7_7	C9	+1.5V_1	D9	Sp7_4	E9	Sp7_5
A10	Sp7_10	B10	Sp7_11	C10	+1.5V_1	D10	Sp7_8	E10	Sp7_9
A11	Sp7_14	B11	Sp7_15	C11	Sp7_12	D11	Sp7_13	E11	Sp7_31
A12	Sp7_19	B12	Sp7_20	C12	Sp7_16	D12	Sp7_17	E12	Sp7_18
A13	Sp7_24	B13	Sp7_25	C13	Sp7_21	D13	Sp7_22	E13	Sp7_23
A14	Sp7_29	B14	Sp7_30	C14	Sp7_26	D14	Sp7_27	E14	Sp7_28
A15	Sp4_2	B15	Sp4_3	C15	GND	D15	Sp4_0	E15	Sp4_1
A16	Sp4_6	B16	Sp4_7	C16	GND	D16	Sp4_4	E16	Sp4_5
A17	Sp4_10	B17	Sp4_11	C17	GND	D17	Sp4_8	E17	Sp4_9
A18	Sp4_31	B18	Sp4_14	C18	Sp4_15	D18	Sp4_12	E18	Sp4_13
A19	Sp4_18	B19	Sp4_19	C19	Sp4_20	D19	Sp4_16	E19	Sp4_17
A20	Sp4_23	B20	Sp4_24	C20	Sp4_25	D20	Sp4_21	E20	Sp4_22
A21	Sp4_28	B21	Sp4_29	C21	Sp4_30	D21	Sp4_26	E21	Sp4_27
A22	Sp9_2	B22	Sp9_3	C22	+1.5V_1	D22	Sp9_0	E22	Sp9_1
A23	Sp9_6	B23	Sp9_7	C23	+1.5V_1	D23	Sp9_4	E23	Sp9_5
A24	Sp9_10	B24	Sp9_11	C24	+1.5V_1	D24	Sp9_8	E24	Sp9_9
A25	Sp9_14	B25	Sp9_15	C25	Sp9_12	D25	Sp9_13	E25	Sp9_31

Table 9: Pin assignment of the X26 [4] backplane connector

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	Sp9_19	B1	Sp9_20	C1	Sp9_16	D1	Sp9_17	E1	Sp9_18
A2	Sp9_24	B2	Sp9_25	C2	Sp9_21	D2	Sp9_22	E2	Sp9_23
A3	Sp9_29	B3	Sp9_30	C3	Sp9_26	D3	Sp9_27	E3	Sp9_28
A4	Sp2_2	B4	Sp2_3	C4	GND	D4	Sp2_0	E4	Sp2_1
A5	Sp2_6	B5	Sp2_7	C5	GND	D5	Sp2_4	E5	Sp2_5
A6	Sp2_10	B6	Sp2_11	C6	GND	D6	Sp2_8	E6	Sp2_9
A7	Sp2_31	B7	Sp2_14	C7	Sp2_15	D7	Sp2_12	E7	Sp2_13
A8	Sp2_18	B8	Sp2_19	C8	Sp2_20	D8	Sp2_16	E8	Sp2_17
A9	Sp2_23	B9	Sp2_24	C9	Sp2_25	D9	Sp2_21	E9	Sp2_22
A10	Sp2_28	B10	Sp2_29	C10	Sp2_30	D10	Sp2_26	E10	Sp2_27
A11	Sp11_2	B11	Sp11_3	C11	+1.5V_1	D11	Sp11_0	E11	Sp11_1
A12	Sp11_6	B12	Sp11_7	C12	+1.5V_1	D12	Sp11_4	E12	Sp11_5
A13	Sp11_10	B13	Sp11_11	C13	+1.5V_1	D13	Sp11_8	E13	Sp11_9
A14	Sp11_14	B14	Sp11_15	C14	Sp11_12	D14	Sp11_13	E14	Sp11_31
A15	Sp11_19	B15	Sp11_20	C15	Sp11_16	D15	Sp11_17	E15	Sp11_18
A16	Sp11_24	B16	Sp11_25	C16	Sp11_21	D16	Sp11_22	E16	Sp11_23
A17	Sp11_29	B17	Sp11_30	C17	Sp11_26	D17	Sp11_27	E17	Sp11_28
A18	Ms_to_ccb0	B18	Ms_to_ccb1	C18	GND	D18	Ms_l1a_req	E18	Ms_cfgdone
A19	W6_0	B19	W6_1	C19	GND	D19	W7_0	E19	W7_1
A20	W5_0	B20	W5_1	C20	GND	D20	W8_0	E20	W8_1

A21	W4_0	B21	W4_1	C21	GND	D21	W9_0	E21	W9_1
A22	W3_0	B22	W3_1	C22	GND	D22	W10_0	E22	W10_1
A23	W2_0	B23	W2_1	C23	GND	D23	W11_0	E23	W11_1
A24	W1_0	B24	W1_1	C24	GND	D24	W12_0	E24	W12_1
A25		B25		C25		D25		E25	

3. Interface to Global Muon Trigger and Output Lookup Table RAM

The interface to the GMT receiver module is based on proposal [5]. The MS-to-GMT data format is shown in Table 10. All signals representing one muon pattern, will be transmitted over twisted pair cable using 68-pin SCSI-3 connectors. Four such connectors are placed on the front panel of the MS. All four selected muons are transmitted at 40 Mhz in ranked order, with connector 1 for the Muon_1 (1st best), connector 2 for Muon_2 (2nd best) and so on. When there are no selected muons, the MS sends Pt[4..0]=Quality[2..0]=0. The SN75LVDS387/LVDT386 chipset from Texas Instruments is being used. Pin assignment of the connector is given in Table 11.

For testing purposes there is one 68-pin SCSI-3 connector and two SN75LVT386 receivers on the MS board. One cable out of four directed to GMT can be plugged into this connector and data saved into FIFO_D buffer (see section 5 for more details). This feature will allow to test the GMT connection even if the GMT receiver module is not available.

Table 10: MS-to-GMT Data Format (per one muon)

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Eta0	**Quality[2..0]**			**Pt[4..0]**					**Phi[7..0]**							
33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17
G	**G**	**Clk**	**G**	**SE**	**Bc0**	**Bx2**	**Bx1**	**Bx0**	**VC**	**C**	**HL**	**Eta[5..1]**				

HL – Halo Muon (0 = "positive" endcap)
VC – Valid Charge
Bx[2..0] – three least significant bits of bunch crossing counter
Bc0 - Bunch Crossing Zero Flag
SE – Synchronization Error, S – sign (=charge) (1 – negative, 0 – positive)
Clock – 40Mhz synchronizing clock, G – Ground
Notes: 1) Pt[4..0] and Quality[2..0] are sent inverted, all other bits are not inverted.
2) For empty candidates (if Pt=0), all bits from 16 to 24 are set to "0", Phi[7..0]="1", Pt[4..0]="1" (after inversion), Quality[2..0]="1" (after inversion)

Table 11: MS-to-GMT Cable Interface (one muon per cable)

Bit	Pin	Signal	Pin	Signal
0	1	Phi_0+	35	Phi_0-
1	2	Phi_1+	36	Phi_1-
2	3	Phi_2+	37	Phi_2-
3	4	Phi_3+	38	Phi_3-
4	5	Phi_4+	39	Phi_4-
5	6	Phi_5+	40	Phi_5-
6	7	Phi_6+	41	Phi_6-
7	8	Phi_7+	42	Phi_7-
8	9	Pt_0+	43	Pt_0-
9	10	Pt_1+	44	Pt_1-
10	11	Pt_2+	45	Pt_2-

11	12	Pt_3+	46	Pt_3-
12	13	Pt_4+	47	Pt_4-
13	14	Quality_0+	48	Quality_0-
14	15	Quality_1+	49	Quality_1-
15	16	Quality_2+	50	Quality_2-
16	17	Eta_0+	51	Eta_0-
17	18	Eta_1+	52	Eta_1-
18	19	Eta_2+	53	Eta_2-
19	20	Eta_3+	54	Eta_3-
20	21	Eta_4+	55	Eta_4-
21	22	Eta_5+	56	Eta_5-
22	23	HL+	57	HL-
23	24	C+	58	C-
24	25	VC+	59	VC-
25	26	BX0+	60	BX0-
26	27	BX1+	61	BX1-
27	28	BX2+	62	BX2-
28	29	BC0+	63	BC0-
29	30	SyncEr+	64	SyncEr-
30	31	GND	65	GND
31	32	40Mhz Clock+	66	40Mhz Clock-
32	33	GND	67	GND
33	34	GND	68	GND

Block diagram of the output data conversion for one muon is shown on Fig 2. Each LUT is implemented inside the main FPGA and available for read and write over VME.

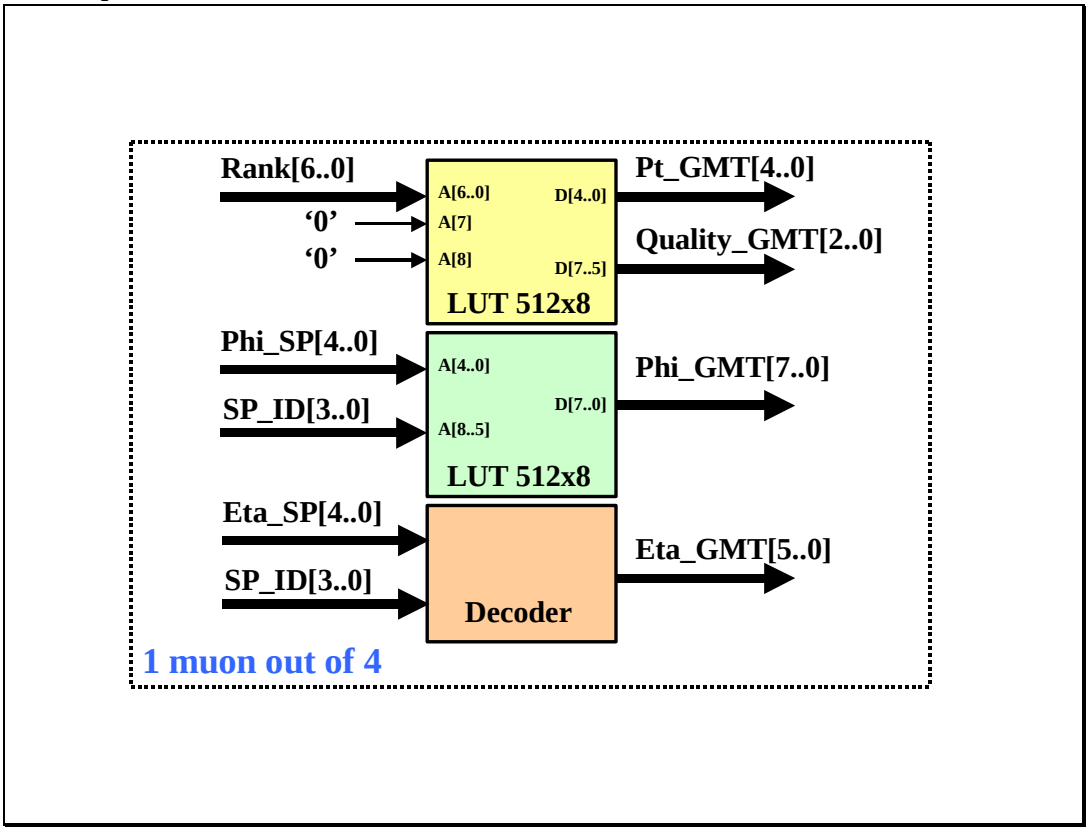

Figure 2: Block Diagram of the Output Data Conversion Scheme

More details about access to LUT are shown in Table 12. Access to all LUT RAMs is available from VME over lines D0-D7 (Phi LUT) and D8-D15 (Rank LUT). All addesses are listed in Table 12. The SP_ID[3..0] represent the physical number of each SP in the TF crate. SP_ID=1 for SP1, SP_ID=2 for SP 2 and so on.

Table 12: Access to LUT RAMs from VME

Rank LUT, 512*8 bit		**Phi LUT, 512*8 bit**	
Address	Data	Address	Data
A0 = Rank[0]	D0 = Pt[0] (VME D8 line)	A0 = Phi_SP[0]	D0 = Phi_GMT[0] (VME D0 line)
A1 = Rank[1]	D1 = Pt[1] (VME D9 line)	A1 = Phi_SP[1]	D1 = Phi_GMT[1] (VME D1 line)
A2 = Rank[2]	D2 = Pt[2] (VME D10 line)	A2 = Phi_SP[2]	D2 = Phi_GMT[2] (VME D2 line)
A3 = Rank[3]	D3 = Pt[3] (VME D11 line)	A3 = Phi_SP[3]	D3 = Phi_GMT[3] (VME D3 line)
A4 = Rank[4]	D4 = Pt[4] (VME D12 line)	A4 = Phi_SP[4]	D4 = Phi_GMT[4] (VME D4 line)
A5 = Rank[5]	D5 = Quality[0] (VME D13 line)	A5 = SP_ID[0]	D4 = Phi_GMT[5] (VME D5 line)
A6 = Rank[6]	D6 = Quality[1] (VME D14 line)	A6 = SP_ID[1]	D6 = Phi_GMT[6] (VME D6 line)
A7 = 0	D7 = Quality[2] (VME D15 line)	A7 = SP_ID[2]	D7 = Phi_GMT[7] (VME D7 line)
A8 = 0		A8 = SP_ID[3]	

3.1. Rank and Phi Look-Up Tables and Eta Decoder

7-bit Rank[6..0] from Sector Processors is already separated into Pt[4..0] and Quality[1..0] fields [5]. The upper two address bits are “0”. So each Rank LUT outputs the data equal to the value on address bus. At this moment it is proposed that the Quality[2]=0.

We assume that SP1-SP6 belong to “positive” endcap of the CSC system, and SP7-SP12 belong to “negative” endcap. Then, based on proposal [4] the Eta decoder performs the following decoding:

- for SP1-SP6: Eta_GMT[4..0] = Eta_SP[4..0], Eta_GMT[5] = 0;
- for SP7-SP12: Eta_GMT[4..0] = Eta_SP[4..0], Eta_GMT[5] = 1.

Sector 1 of the CSC system starts at phi=15 degrees, which is equal to bin 6 (with the binning in 2.5 degree intervals). Each sector covers 60 degrees, so the LUT would add 6 to Phi value for sector 1 and 7, 6+24 to Phi value for sector 2 and 8 and so on. The Phi LUT content can be summarized as:

- for SP1 and SP7: Phi_GMT[7..0] = Phi_SP[4..0] + 6
- for SP2 and SP8: Phi_GMT[7..0] = Phi_SP[4..0] + 30
- for SP3 and SP9: Phi_GMT[7..0] = Phi_SP[4..0] + 54
- for SP4 and SP10: Phi_GMT[7..0] = Phi_SP[4..0] + 78
- for SP5 and SP11: Phi_GMT[7..0] = Phi_SP[4..0] + 102
- for SP6 and SP12: Phi_GMT[7..0] = Phi_SP[4..0] + 126

4. VME Interface

The MS decodes A24 addresses when the code on address lines A[23..19] is equal to the 5-bit geographical address of the slot in a crate where it is located. This mode requires using of J1 part of the VME64x backplane. In case of using the TF custom backplane, the

MS slot is 14, and the base geographical address is 700000(hex). The MS recognizes AM codes 39(hex) and 3D(hex). Decoded addresses and VME commands are listed in Table 13. The MS does not respond to byte-addressing modes, so all valid addresses must be even numbers.

Table 13: Decoded VME addresses

Address (hex)	Access	Function
XCR3128XL PLD		
700000…70000E	Read/Write	SCANPSC100F JTAG Controller
700010	Write*	Reset SCANPSC100F controller
700012	Read/Write	CSR4 (see Table 22)
700014	Read	CSR3 (see Table 21)
700016	Write*	Generate 400 ns Hard Reset pulse to main FPGA
700018	Write*	Generate "Reset" pulse (FIFOs etc) to main FPGA
XC2V4000-5FF1152C FPGA		
700100	Read/Write	FIFO_A1[15..0]. Corresponds to SP1
700102	Read/Write	FIFO_A1[31..16]. Corresponds to SP1
700104	Read/Write	FIFO_A2[15..0]. Corresponds to SP2
700106	Read/Write	FIFO_A2[31..16]. Corresponds to SP2
700108	Read/Write	FIFO_A3[15..0]. Corresponds to SP3
70010A	Read/Write	FIFO_A3[31..16]. Corresponds to SP3
70010C	Read/Write	FIFO_A4[15..0]. Corresponds to SP4
70010E	Read/Write	FIFO_A4[31..16]. Corresponds to SP4
700110	Read/Write	FIFO_A5[15..0]. Corresponds to SP5
700112	Read/Write	FIFO_A5[31..16]. Corresponds to SP5
700114	Read/Write	FIFO_A6[15..0]. Corresponds to SP6
700116	Read/Write	FIFO_A6[31..16]. Corresponds to SP6
700118	Read/Write	FIFO_A7[15..0]. Corresponds to SP7
70011A	Read/Write	FIFO_A7[31..16]. Corresponds to SP7
70011C	Read/Write	FIFO_A8[15..0]. Corresponds to SP8
70011E	Read/Write	FIFO_A8[31..16]. Corresponds to SP8
700120	Read/Write	FIFO_A9[15..0]. Corresponds to SP9
700122	Read/Write	FIFO_A9[31..16]. Corresponds to SP9
700124	Read/Write	FIFO_A10[15..0]. Corresponds to SP10
700126	Read/Write	FIFO_A10[31..16]. Corresponds to SP10
700128	Read/Write	FIFO_A11[15..0]. Corresponds to SP11
70012A	Read/Write	FIFO_A11[31..16]. Corresponds to SP11
70012C	Read/Write	FIFO_A12[15..0]. Corresponds to SP12
70012E	Read/Write	FIFO_A12[31..16]. Corresponds to SP12
700130	Read/Write	FIFO_B1[15..0]. Corresponds to 1st best muon transmitted to GMT
700132	Read/Write	FIFO_B1[31..16]. Corresponds to 1st best muon transmitted to GMT
700134	Read/Write	FIFO_B2[15..0]. Corresponds to 2nd best muon transmitted to GMT
700136	Read/Write	FIFO_B2[31..16]. Corresponds to 2nd best muon transmitted to GMT
700138	Read/Write	FIFO_B3[15..0]. Corresponds to 3rd best muon transmitted to GMT
70013A	Read/Write	FIFO_B3[31..16]. Corresponds to 3rd best muon transmitted to GMT
70013C	Read/Write	FIFO_B4[15..0]. Corresponds to 4th best muon transmitted to GMT
70013E	Read/Write	FIFO_B4[31..16]. Corresponds to 4th best muon transmitted to GMT
700140	Read/Write	FIFO_C1[15..0]. Corresponds to 1st best muon from the sorter output
700142	Read/Write	FIFO_C1[31..16].Corresponds to 1st best muon from the sorter output
700144	Read/Write	FIFO_C2[15..0]. Corresponds to 2nd best muon from the sorter output
700146	Read/Write	FIFO_C2[31..16].Corresponds to 2nd best muon from the sorter output
700148	Read/Write	FIFO_C3[15..0]. Corresponds to 3rd best muon from the sorter output
70014A	Read/Write	FIFO_C3[31..16].Corresponds to 3rd best muon from the sorter output
70014C	Read/Write	FIFO_C4[15..0]. Corresponds to 4th best muon from the sorter output

70014E	Read/Write	FIFO_C4[31..16].Corresponds to 4th best muon from the sorter output
700150	Read/Write	FIFO_D[15..0]. Input FIFO (GMT connection)
700152	Read/Write	FIFO_D[31..16]. Input FIFO (GMT connection)
700158	Read/Write	CSR0 (general purpose, main FPGA). See Table 18.
70015A	Read	CSR1 (FIFO full/empty status, main FPGA). See Table 19.
70015C	Read	CSR2 (date of the firmware version, main FPGA). See Table 20.
70015E	Write*	Transmit 255 words (510 frames) of data from all FIFO_A buffers in "Test" mode
700160	Write**	Set up fine phase adjustment for DCM1 (main clock).
700162	Write**	Set up fine phase adjustment for DCM2 (output clock to GMT).
700164	Write*	Reset PSDONE status bits from DCM1 and DCM2
700166		
700168	Read	CSR5 (DCM status register, see Table 23)
70016A		
70016E		
700400-7007FE	Read/Write	Rank and Phi Look-Up Tables, Muon_1 (see Table 12)
700800-700BFE	Read/Write	Rank and Phi Look-Up Tables, Muon_2 (see Table 12)
700C00-700FFE	Read/Write	Rank and Phi Look-Up Tables, Muon_3 (see Table 12)
701000-7013FE	Read/Write	Rank and Phi Look-Up Tables, Muon_4 (see Table 12)

* Write any data.

** Write "1" to increase phase shift by 1 bit. Write "0" to decrease phase shift by 1 bit.

5. FIFO Buffers

Four groups of FIFO Buffers (FIFO_A, FIFO_B, FIFO_C and FIFO_D) are implemented in the main FPGA in order to test the MS internal functionality and its communications with the SP and GMT (Figure 3). All buffers are 511-word deep and available from VME for read and write (Table 13). Since three muon patterns are packed into FIFO_A in two frames, each FIFO_A effectively comprises 255 patterns. Each buffer A represents data corresponding to one SP board, or three muon patterns. Its format is shown in Table 14. FIFO_A1 corresponds to SP1, FIFO_A2 corresponds to SP2 and so on. In a "Test" mode the test patterns representing 36 muons can be send out simultaneously from all FIFO_A buffers at 80Mhz upon specific VME command (note the last word to be loaded into every FIFO_A must be "0" for proper operation). They pass through the sorter that selects four best patterns and transmits them to GMT and FIFO_B.

The FIFO_B format is shown in Table 15. In "Trigger" mode the selected patterns from SP's act as a data sources. The outputs from the sorter (before LUT conversion) can be stored inside FIFO_C. Its data format is shown in Table 16. FIFO_B and FIFO_C operate at 40Mhz (as well as outputs to GMT). FIFO_D format is shown in Table 17. An external cable can connect one of the front panel connectors to on-board connector P12. Thus an output data representing one selected muon can be stored in FIFO_D instead of sending to GMT. Data is loaded into FIFO_D only if at least one out of seven Pt[4..0]+Quality[1..0] bits is non-zero.

Table 14: FIFO_A Data Format

FIFO_A Frame 1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Phi_Muon_2[4..0]					Eta_Muon_1[4..0]					Phi_Muon_1[4..0]				
FIFO_A Frame 1															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SE	Bc0	Eta_Muon_3[4..0]					Phi_Muon_3[4..0]					Eta_Muon_2[4..0]			
FIFO_A Frame 2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Rank_Muon_2[6..0]						HL	C	VC	Rank_Muon_1[6..0]						
FIFO_A Frame 2															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SP	Bx0	HL	C	VC	Rank_Muon_3[6..0]							HL	C	VC	

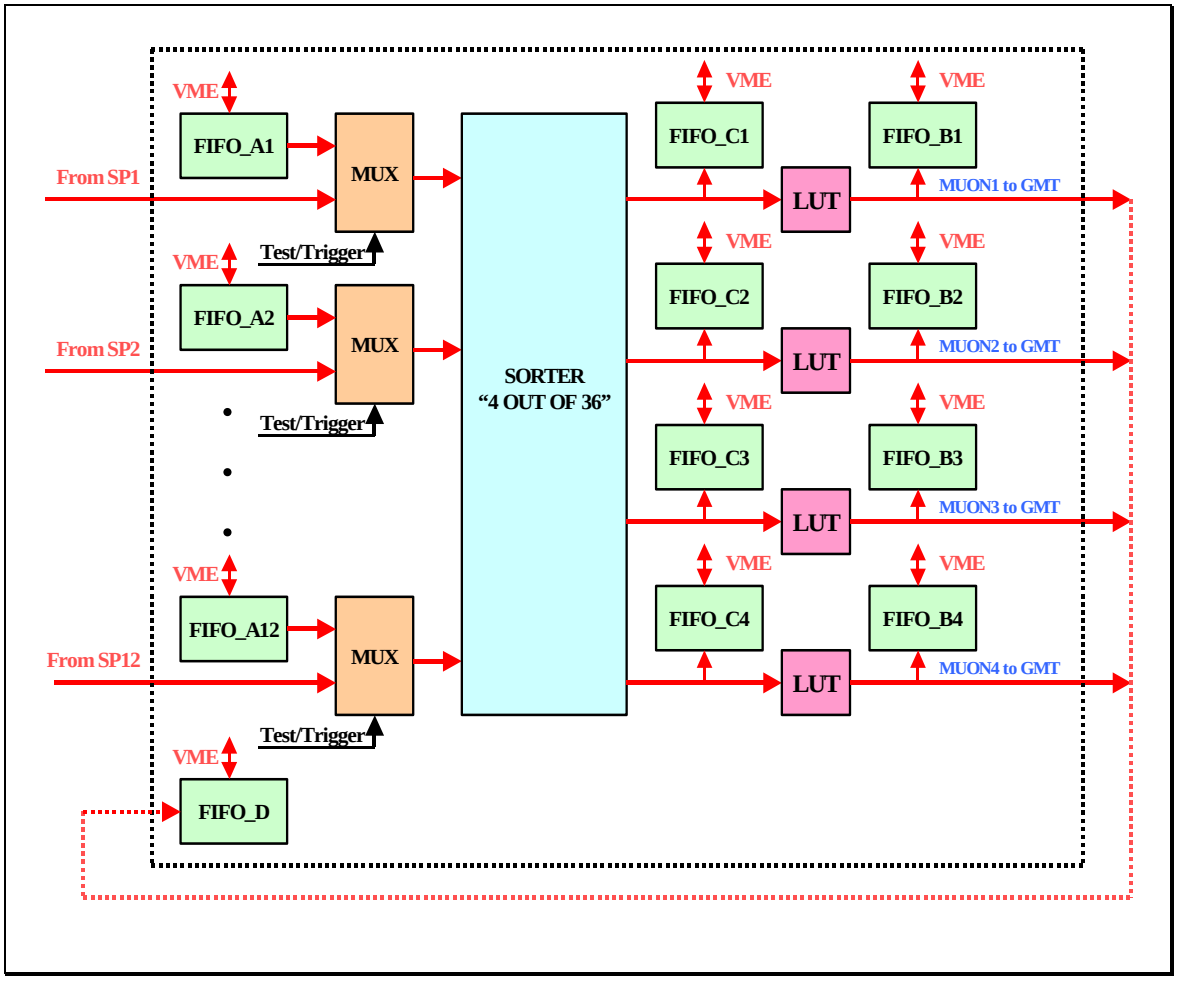

Figure 3: Block Diagram of FIFO Buffers

Table 15: FIFO_B Data Format

FIFO_B															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Quality[2..0]			**Pt[4..0]**					**Phi[7..0]**							
FIFO_B															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
"0"	**P***	**SE**	**Bc0**	**Bx2**	**Bx1**	**Bx0**	**VC**	**C**	**HL**	**Eta[5..0]**					

Note1. BX[2..0] and SE bits are entering the FIFO_B after masking (see CSR0[6..5]). See also notes 1) and 2) to Table 10.
Note 2. (*) Parity (P) is calculated for bits [29..0]. P="1" if the number of "1" is even.

Table 16: FIFO_C Data Format

FIFO_C															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Eta0	**Phi[4..0]**					**HL**	**C**	**VC**	**Rank[6..0]**						
FIFO_C															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
"0"	**"0"**	**"0"**	**"0"**	**ID3**	**ID2**	**ID1**	**ID0**	**SE**	**Bc0**	**SP**	**Bx0**	**Eta[4..1]**			

ID[3..0] bits correspond to physical address (1 to 12, counting from the very left (slot 6) Sector Processor) of the particular SP in the TF crate.

Table 17: FIFO_D Data Format

FIFO_D															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Quality[2..0]			**Pt[4..0]**					**Phi[7..0]**							
FIFO_D															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
"0"	**"0"**	**SE**	**Bc0**	**Bx2**	**Bx1**	**Bx0**	**VC**	**C**	**HL**	**Eta[5..0]**					

Note: see notes 1) and 2) to Table 10.

One important feature of all FIFO_B and FIFO_C buffers is that the data from FIFO_A ("Test" mode) or SP's ("Trigger" mode) can be saved in FIFO_B or FIFO_C only if there is at least one valid muon pattern. This allows acquiring into FIFO_B and FIFO_C the data, representing only valid patterns. The non-zero 7-bit rank indicator from the **first best selected muon after sorting** acts as "write enable" signal for all FIFO_C buffers. The non-zero 7-bit Pt[4..0]+Quality[1..0] value of the **first best selected muon after LUT** conversion acts as "write enable" signal for all FIFO_B buffers. This means that if there is just one valid pattern coming after sorting from FIFO_A or SP, it will be stored in FIFO_C1 and "0" will be written into other FIFO_C buffers. The same is true for FIFO_B buffers. This assures that all four FIFO_B and all four FIFO_C buffers will contain an equal number of words inside. As for VME access, any data can be loaded and read back out of any FIFO buffer independently.

FULL and EMPTY flags (common to all FIFO_A[12..1], FIFO_B[4..1], FIFO_C[4..1] and FIFO_D buffers) are available for read from CSR1. After asynchronous FIFO reset all these flags are active "1".

6. Control and Status Registers (CSR)

The formats of CSR<0-5> are shown in Tables 18-23.

Table 18: CSR0 (inside the main FPGA)

Bit	Function
0 (R/W)	FPGA_Mode (Trigger mode if "0", Test mode (FIFO_A is a source of data) if "1")
1(R/W)	BXN[0] offset. Being loaded into BXN counter on L1Reset
2 (R/W)	BXN[1] offset. Being loaded into BXN counter on L1Reset
3 (R/W)	BXN[2] offset. Being loaded into BXN counter on L1Reset
4 (R/W)	BXN[3] offset. Being loaded into BXN counter on L1Reset
5 (R/W)	MASKSP (Masks SE bits from all selected patterns (enabled if "1" and disabled if "0")
6 (R/W)	MASKCOMP (Masks all outputs of BXN comparators (enabled if "1" and disabled if "0")
7 (R/W)	MASKER (Masks transmission of BX0 bit from selected muons to GMT (enabled if "1" and disabled if "0"). Bits BXN[2..1]=0.
8 (R/W)	MASKBXN (Masks transmission of BXN[2..0] bits from internal bunch crossing counter to GMT (enabled if "1"and disabled if "0")
9 (R/W)	Enable MS_L1A_Request generation to CCB (enabled if "1" and disabled if "0")
10 (R/W)	-
11 (R/W)	-
12 (R/W)	Delay of all "winner" bits to SP, LSB
13 (R/W)	Delay of all "winner" bits to SP
14 (R/W)	Delay of all "winner" bits to SP
15 (R/W)	Delay of all "winner" bits to SP, MSB

Table 19: CSR1 (inside the main FPGA, FIFO status outputs)

Bit and access	Function
0 (R)	FIFO_A FULL. Active "1" if at least one out of 12 FIFO_A buffers is full
1(R)	FIFO_A EMPTY. Active "1" if ALL 12 FIFO_A buffers are empty. Also "1" after reset
2 (R)	FIFO_B FULL. Active "1" if at least one out of four FIFO_B buffers is full
3 (R)	FIFO_B EMPTY. Active "1" if ALL four FIFO_B buffers are empty. Also "1" after reset
4 (R)	FIFO_C FULL. Active "1" if at least one out of four FIFO_C buffers is full
5 (R)	FIFO_C EMPTY. Active "1" if ALL four FIFO_C buffers are empty. Also "1" after reset
6 (R)	FIFO_D FULL. Active "1" if FIFO_D is full
7 (R)	FIFO_D EMPTY. Active "1" if FIFO_D is empty. Also "1" after reset
8 (R)	"0"
9 (R)	"0"
10 (R)	"0"
11 (R)	"0"
12 (R)	"0"
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

Table 20: CSR2 (inside main FPGA, date of the current firmware version)

Bit and access	Function
0 (R)	Day, LSB
1(R)	Day
2 (R)	Day
3 (R)	Day
4 (R)	Day, MSB
5 (R)	Month, LSB
6 (R)	Month
7 (R)	Month
8 (R)	Month, MSB
9 (R)	Year, LSB (*)
10 (R)	Year (*)
11 (R)	Year, MSB (*)
12..15 (R)	"0"

(*) The code at CSR2<11..9> should be added to 2000 to get an actual year. For example, CSR2=1252(dec) corresponds to July 4, 2002.

Table 21: CSR3 (inside control CPLD)

Bit and access	Function
0 (R)	FPGA Configuration Done and DLL locked (Active "1")
1(R)	-
2 (R)	-
3 (R)	-
4 (R)	-
5 (R)	-
6 (R)	-
7 (R)	-
8 (R)	-
9 (R)	-
10 (R)	-
11 (R)	-
12 (R)	-
13 (R)	-
14 (R)	-
15 (R)	-

Table 22: CSR4 (inside control CPLD)

Bit and access	Function
0 (R/W)	Enable (when "1") or disable (when "0") the JTAG SCANPSC100F controller. Set to "0" after power up.
1(R/W)	-
2 (R/W)	-
3 (R/W)	-
4 (R/W)	-
5 (R/W)	-
6 (R/W)	-
7 (R/W)	-
8 (R/W)	-
9 (R/W)	-
10 (R/W)	-
11 (R/W)	-

12 (R/W)	-
13 (R/W)	-
14 (R/W)	-
15 (R/W)	-

Table 23: CSR5 (inside main FPGA, DCM status bits)

Bit and access	Function
0 (R)	PSDONE status from DCM1
1(R)	PSDONE status from DCM2
2 (R)	STATUS[0] from DCM1
3 (R)	STATUS[1] from DCM1
4 (R)	STATUS[2] from DCM1
5 (R)	STATUS[0] from DCM2
6 (R)	STATUS[1] from DCM2
7 (R)	STATUS[2] from DCM2
8 (R)	"0"
9 (R)	"0"
10 (R)	"0"
11 (R)	"0"
12 (R)	"0"
13 (R)	"0"
14 (R)	"0"
15 (R)	"0"

7. Mezzanine Board and JTAG Access to FPGA and EPROM

A mezzanine card designed for the SP board is being used. It comprises one Xilinx XC2V4000-5FF1152C FPGA and five XC18V04 EPROMs, all accessible over JTAG. Four EPROMs are needed for the chosen FPGA. An FPGA and all EPROMs can be accessed over Xilinx Parallel Cable IV using 14-pin connector P10. Pin assignment is shown in Table 24. In addition to that a fast JTAG access to FPGA and EPROMs from the VME bus is possible using 8-bit Fairchild SCANPSC100F [7] controller. There is a Xilinx CoolRunner XCR3128XL CPLD [8] that acts as a VME interface for this JTAG controller. The CPLD itself can be programmed over Xilinx Parallel Cable IV (separate 14-pin connector P11). CSR4[0] should be set to "1" in order to enable operation of the SCANPSC100F controller. A software [9] available from the University of Florida can be used to operate the SCANPSC100F controller in a VME crate.

The main 40.08 Mhz clock for the mezzanine card is provided from the MS board. It can be either CCB clock obtained from the backplane (when S1 1-4 is "on" and S1 2-3 is "off") or internal 40.08Mhz clock from an on-board oscillator (when S1 2-3 is "on" and S1 1-4 is "off").

Table 24: Xilinx Parallel Cable IV, connectors P10 and P11

Pin	Signal
1	GND
2	+3.3V
3	GND
4	TMS
5	GND

6	TCK
7	GND
8	TDO (input in respect to target FPGA or CPLD)
9	GND
10	TDI (output in respect to target FPGA or CPLD)
11	GND
12	
13	GND
14	

7. Switches and Fuses

DIP switch S1 is needed to select the source of the master clock. If S1 1-4 is "on", the source is the 40.08 clock from the CCB. If S1 2-3 is "on", the source is on-board quartz oscillator (80.16 Mhz divided by 2). The standard option is when S1 1-4 is "on".

Fuse F5 provides +5V from VME J1 backplane. Fuse F3 provides +1.5V for the mezzanine card from on-board voltage regulator U52. Both are required at any time.

Fuse F4 provides +3.3V power from J1 VME64x backplane while fuse F7 provides +3.3V from on-board voltage regulator U54. Only one (either F7 or F4) should be installed at a time. In case of using VME64x backplane the F4 is recommended**.**

Fuses F1, F2, F6 and F8 provide reference voltages for GTLP transceivers (+1.0V) and GTLP terminators (+1.5V). Fuses F1 and F6 provides these powers from custom Track Finder backplane (only one should be installed at a time) while F2 and F8 provide powers from on-board voltage regulator U53 (only one should be installed at a time). It is recommended to use F1 and F6 when custom Track Finder backplane is being used.

8. Front Panel

There are on the front panel:

- Four 68-pin connectors for communication with GMT receiver;
- Four red LEDs "MUON[1..4] (D1-D4 respectively, with one-shots) that indicate a valid muon patters passing to GMT;
- Green LED "DONE" (D13) indicates that FPGA configuration and initialization done properly and the DLL is locked;
- Yellow LED "TEST" (D6) indicates a "Test" mode (CSR0[0]=1) is active;
- Red LED "JTAG" (D7) indicates access to JTAG from VME using SCANPSC100F;
- Yellow LED "DACK" (D5, with one-shot) indicates an access to MS over VME;
- Green LEDs "+5.0V" (D14), "+3.3V" (D16), "+1.5V" (for FPGA) (D18), "+1.5VA" (D20) (for GTLP terminators) indicate an active on-board powers;
- Red LED "FAEM" (FIFO_A Empty) (D10) indicates that all 12 FIFO_A buffers are empty;
- Red LED "FBEM" (FIFO_B Empty) (D11) indicates that all 4 FIFO_B buffers are empty;

- Red LED “FAFL” (FIFO_A Full) (D8) indicated that at least one out of 12 FIFO_A buffers is full;
- Red LED “FBFL” (FIFO_B Full) (D9) indicates that at least one out of 4 FIFO_B buffers is full;
- Green “CNT” LED (D12). When flashing indicates that 40Mhz clock is provided for the main FPGA.
- Two reserved (D15 and D17) red LED’s.

9. Initialization and Testing Procedures

The initialization and testing procedures include:

1. Make sure the FPGA was configured correctly (read CSR3[0]) after power up.
2. Program CSR0.
3. Send reset to FIFO’s (write any data into address 700018(hex)
4. Read CSR1 and make sure all FIFO’s are empty.
5. Load all LUT’s. Make sure data=0 at the address=0.
6. Load data into FIFO_A[1-12]. Make sure the last two frames written into every FIFO_A buffer are “0”.
7. Start data transmission from all FIFO_A buffers (write any data into address 70015e(hex) or send command=31(hex) from CCB).
8. Read CSR1 and make sure all FIFO_A buffers are empty.
9. Read and check FIFO_C[1..4] buffers until they are empty.
10. Read and check FIFO_B[1..4] buffers until they are empty.
11. Read and check FIFO_D buffers if an external cable is connected for selected output muon.

References

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History

10/15/2002. Initial Release
11/06/2002. Update of Section 7.

11/18/2002. Changes in CSR0 format.
12/06/2002. Major changes in Tables 5..8.
01/23/2003. Changes in Table 5. FIFO_C was added.
01/27/2003. FIFO_D was added.
03/17/2003. Changes in Table 11 and CSR0.
03/20/2003. Section 3.1 was added.
04/09/2003. Section 7 (Switches and Fuses) was added.
04/17/2003: Addresses of the PLD and FPGA (Table 12) were changed.
07/29/2003: CSR4 was modified.
11/05/2003: VME interface was modified. Now the MS responds to geographical addressing only.
11/23/2003: Change format in Table 5.
12/05/2003: Section 1 and Table 13 were updated. CSR5 was added.
04/19/2004: Section 9 was added.
05/04/2004: Minor changes in Section 3 and FIFO_B format