CSC  Muon Sorter

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Muon Sorter Block Diagram

9U * 400 MM BOARD

CCB INTERFACE

SORTER LOGIC

INPUT AND OUTPUT FIFO BUFFERS

Xilinx XC2V4000

VME/JTAG INTERFACE

LVDS DRIVERS

SCSI-3 CONNECTORS

CABLES TO GLOBAL MUON TRIGGER CRATE

MEZZANINE CARD

CUSTOM BACKPLANE

VME J1 BACKPLANE

GTLP TRANSCEIVERS

1st

2nd

3rd

4th
FPGA Design

- **Comprises:**
  - Sorter “4 out of 36” based on 7-bit Rank
  - Output LUT
  - 12 Input and 4 output 32-bit FIFO buffers (255-bit deep)
  - “Winner” logic
  - CCB interface
  - VME interface (A24D16 slave + Geographical Address)

- **Based on** Xilinx XC2V4000-5FF1152C (~60% of FPGA resources are used, ~50Mhz performance using ISE 5.1.03i XST Synthesis)

- **Ghost cancellation logic is not included**

- **Latency – 132 ns**
  - Input latching @ 80MHz and demultiplexing - 1.0 BX
  - Sorting “4 out of 36” and output data merging - 2.5 BX (reduced from 3.0)
  - LUT conversion - 1.0 BX
  - Output data latching - 0.5 BX
  - GTLP-to-LVTTL and LVTTL-to-LVDS conversion - 6 ns
Muon Sorter Output Data Conversion

1 muon out of 4
# MS-to-GMT Data Format

## 32 bits @ 40MHz per each muon

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<th>15</th>
<th>14</th>
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<th>12</th>
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<tr>
<td>CLK</td>
<td>GND</td>
<td>SE</td>
<td>BC0</td>
<td>BX2</td>
<td>BX1</td>
<td>BX0</td>
<td>VC</td>
<td>S</td>
<td>HL</td>
<td>Eta5</td>
<td>Eta4</td>
<td>Eta3</td>
<td>Eta2</td>
<td>Eta1</td>
<td>Eta0</td>
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</table>

- **CLK** - 40Mhz Clock
- **Phi** – Phi Coordinate
- **SE** - Synchronization Error
- **HL** – Halo Muon
- **S** – Muon Sign
- **VC** – Valid Charge (8th bit of Pt LUT output from SP)
- **QU** – Quality
- **BXN** – Bunch Crossing Number
- **Pt** – Momentum
- **Eta** – Eta Coordinate
- **GND** - Ground
**SP Interface**

- Data format, backplane and FPGA pin assignment are completely defined
- 28 SN74GTLPH16912 transceivers and 50 terminator resistor networks will be placed on both sides of the board

**GMT Interface**

- Data format completely defined
- Need to finalize the connector part number. Pin assignment done
- SN74LVDS386/387 LVDS chipset

**JTAG Interface**

- JTAG Access to Xilinx XC2V4000 FPGA
  - From VME using Fairchild SCANPSC100FSC JTAG controller
  - Xilinx Parallel Cable 4 (14-pin connector)
- JTAG Access to Xilinx XCR3128 PLD (VME control logic for SCANPSC100)
  - Xilinx Parallel Cable 4 (separate 14-pin connector)
Front Panel (single width)

- Four 68-pin SCSI-3 connectors (64 mm long each)

- 17 small LEDs
  - 4 winner muons sent to GMT
  - DTACK
  - JTAG access to FPGA from VME
  - FPGA configuration done
  - Test/Trigger Mode
  - Input/Output FIFO status (full/empty)
  - power +5V, +3.3V, +1.5V status
  - 1 reserved
MS Preliminary Cost Estimate

PCB Routing - $8K
PCB Fabrication (3 boards) - $3K
PCB Assembly (3 boards) - $1K
Components - $3K per board *
Mezzanine card fabrication and assembly - $1K per board

Total for 3 boards - $24K ($20K)

* Mainly FPGA. Have 2 free FPGA (donation from Xilinx)
Muon Sorter Design Status and Plans

- Orcad schematic is completed (54 small chips, mostly drivers and receivers). The board is unpopulated, but routing will be complex due to mezzanine connections. 670 out of 782 mezzanine i/o are used.

- Updated specification is available on the web

- FPGA and PLD initial designs done (Xilinx Foundation ISE 5.1.03)

- Have most components in hand (excluding mezzanine connectors and assembled mezzanine cards)

- Ordered 9U Wiener crate. Expect by the end of January

- Ready to start PCB layout (outside vendor)
  - January…February – layout and fabrication (3 boards)
  - March…May – assembly and testing