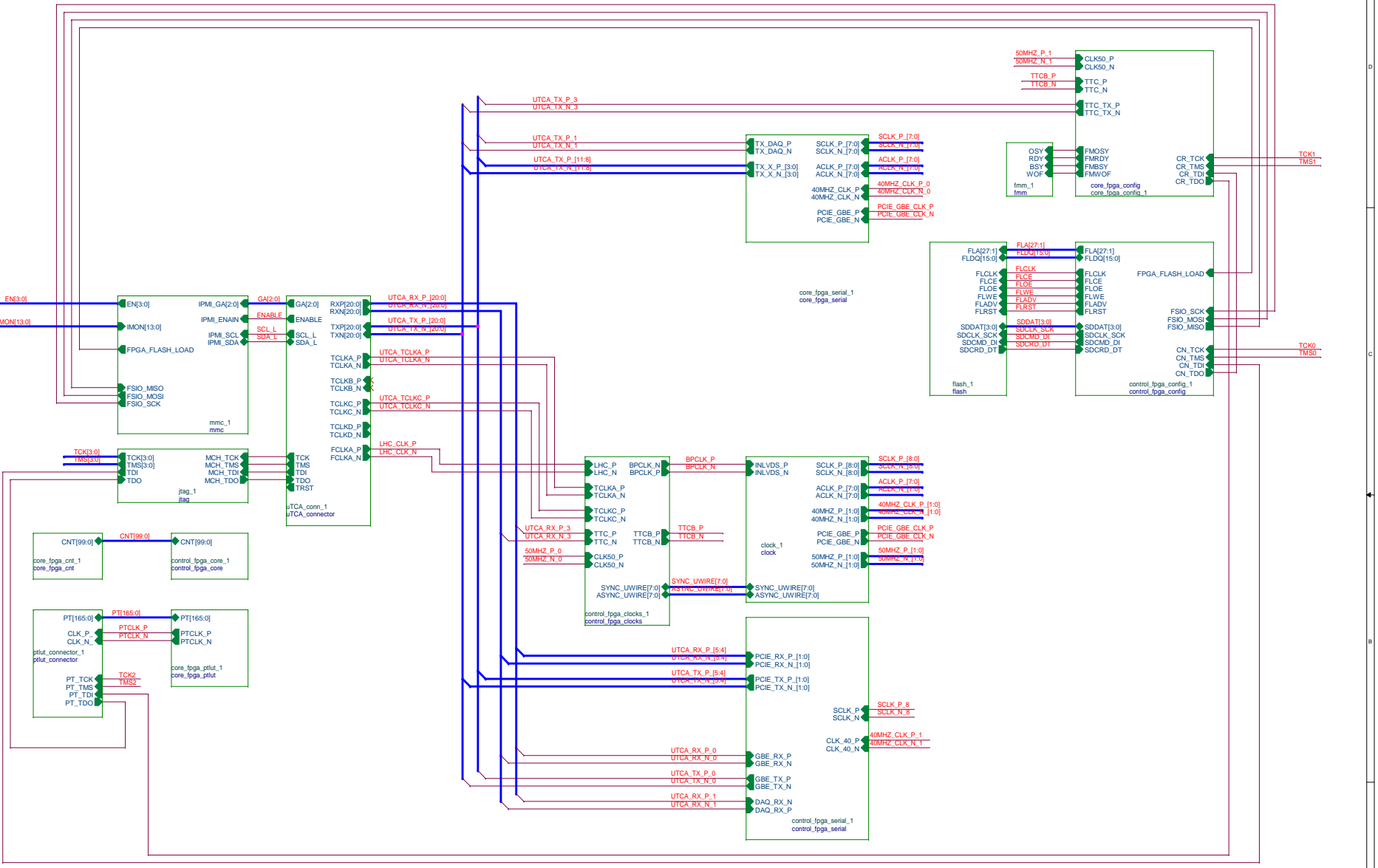
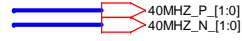
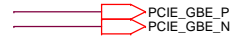
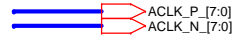
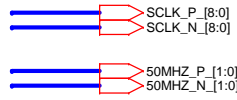


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 custom_bp_grnd
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 core_fpga_power_1
 core_fpga_power
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 control_fpga_unused

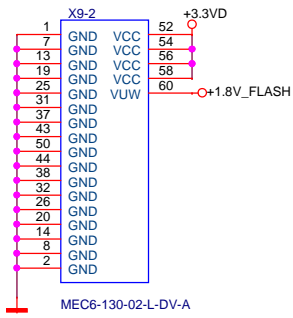
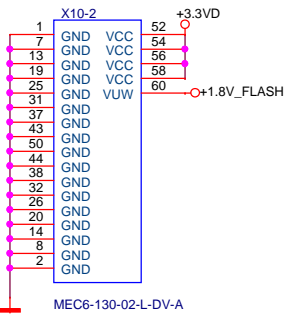
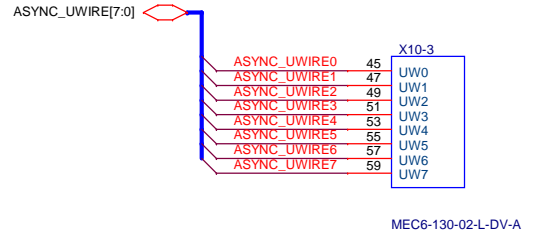
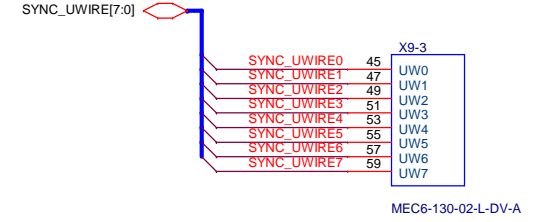
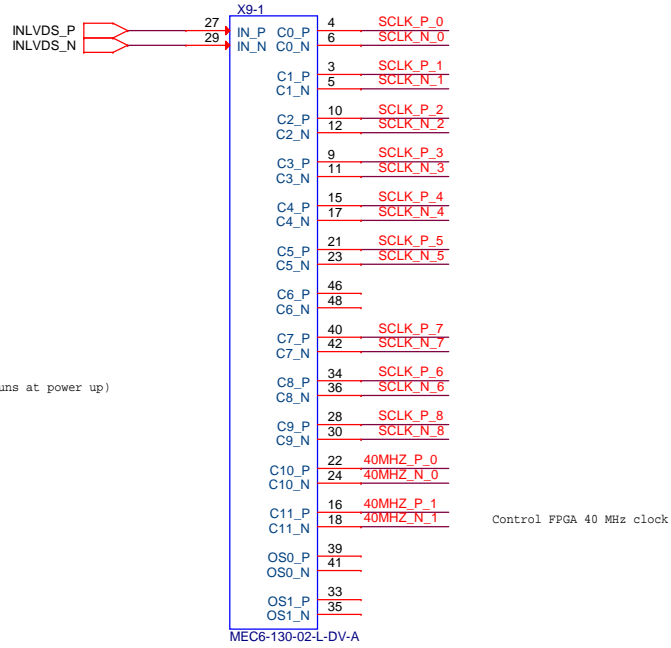
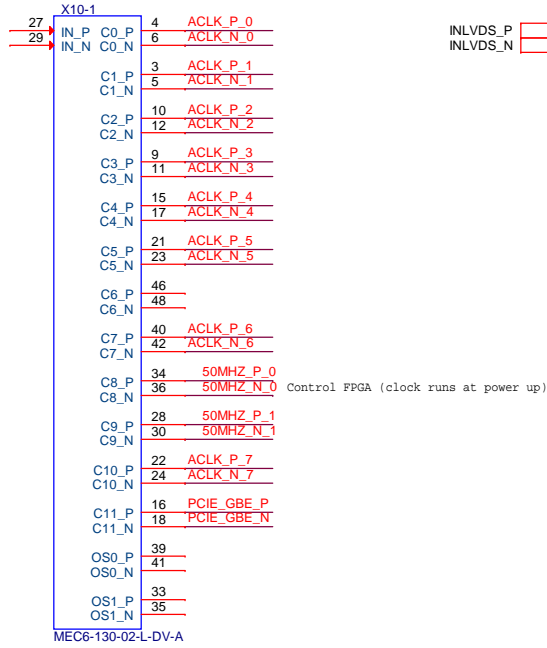
sdram_1
 sdram

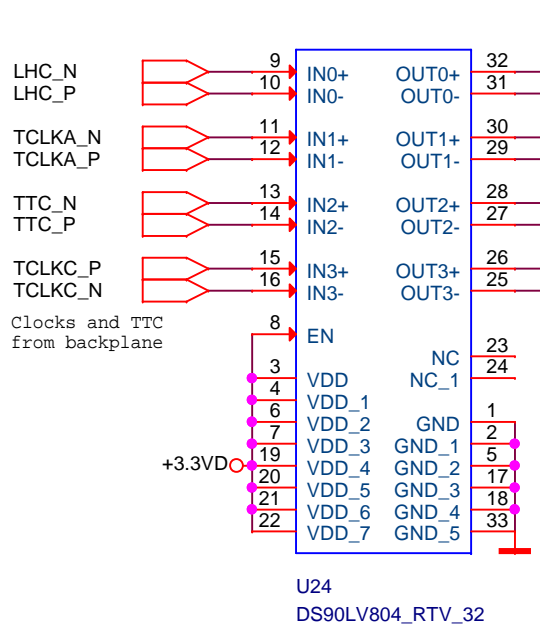
EN[3:0]
 IMON[13:0]
 dc-dc_1
 dc-dc





CONNECTORS FOR CLOCK MODULES





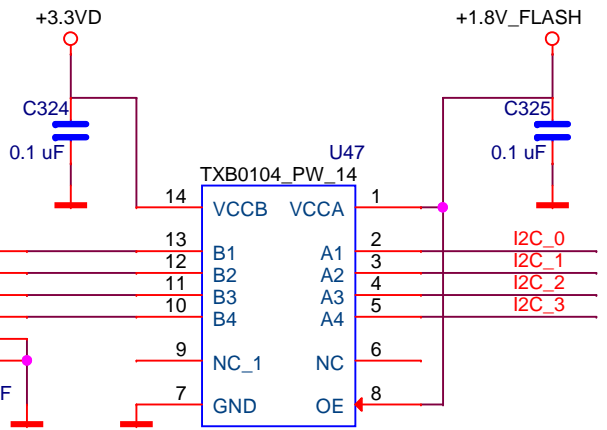
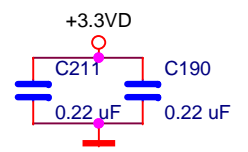
Do not terminate TTC in firmware,
it should be terminated in Core FPGA

Buffered TTC for Core FPGA

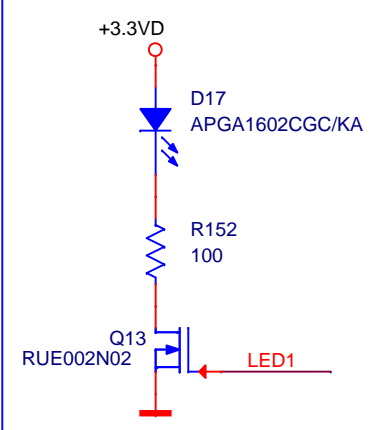
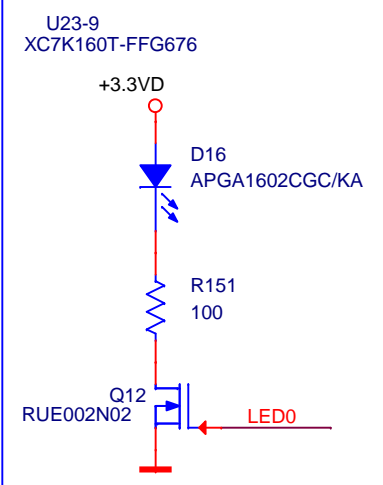
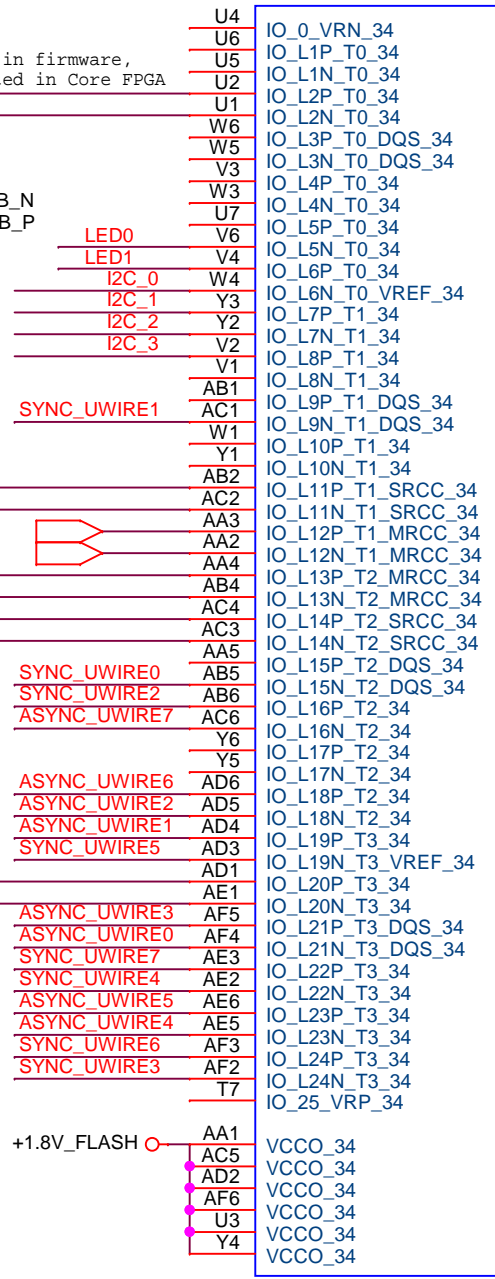
clock derived from async clock

Clock selected for de jittering

LVDS signals coming from backplane
Common Mode Min/Max 0.3/2.1V
Amplitude Min/Max 0.480/0.650V
FPGA would not tolerate that directly
have to use external buffer



Front panel connection to optical board
for accessing optical parts and redrivers

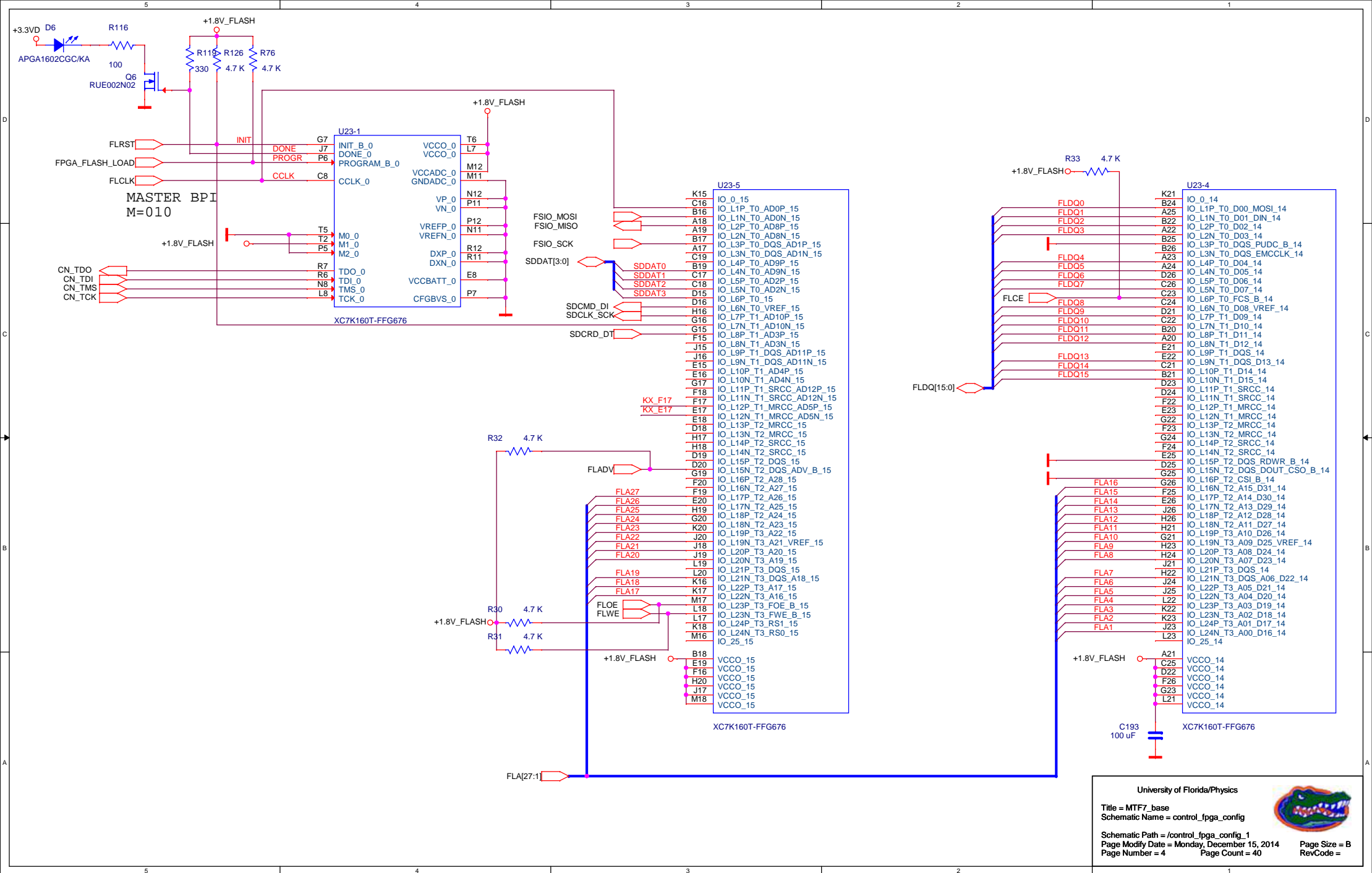


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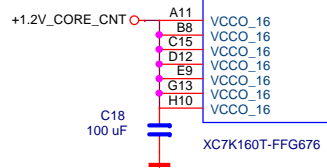
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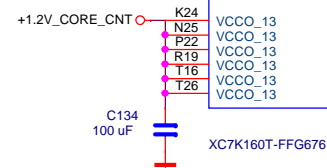
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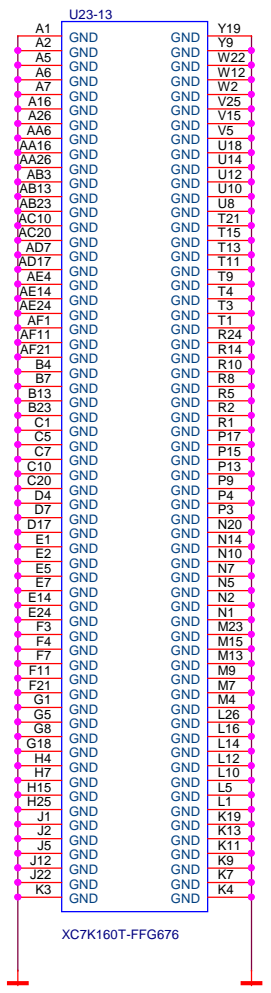
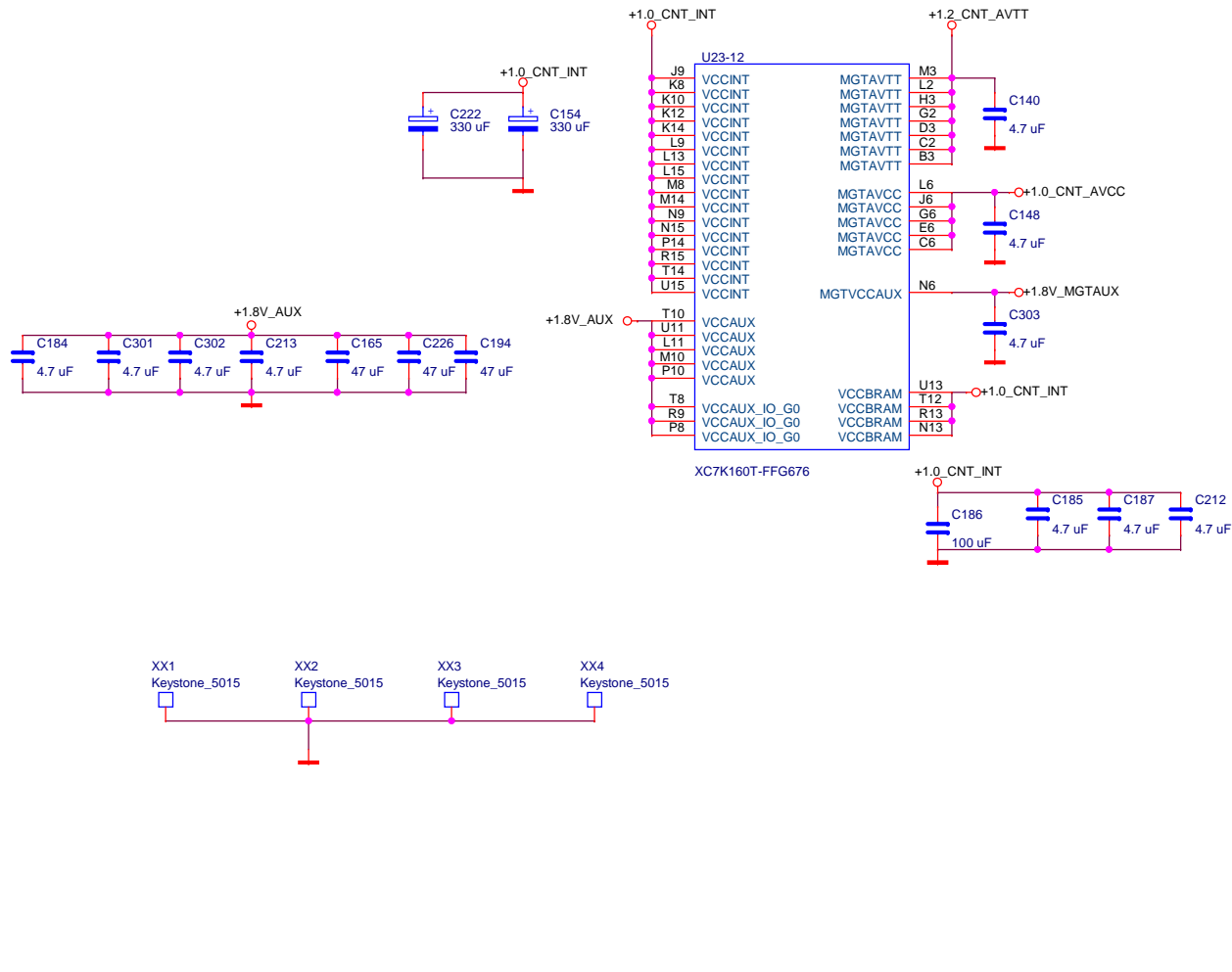
U23-6	
CNT0	J8 IO_0_16
CNT1	H9 IO_L1P_T0_16
CNT2	H8 IO_L1N_T0_16
CNT3	G10 IO_L2P_T0_16
CNT4	G9 IO_L2N_T0_16
CNT5	J13 IO_L3P_T0_DQS_16
CNT6	H13 IO_L3N_T0_DQS_16
CNT7	J11 IO_L4P_T0_16
CNT8	J10 IO_L4N_T0_16
CNT9	H14 IO_L5P_T0_16
CNT10	G14 IO_L5N_T0_16
CNT11	H12 IO_L6P_T0_16
CNT12	H11 IO_L6N_T0_VREF_16
CNT13	F9 IO_L7P_T1_16
CNT14	F8 IO_L7N_T1_16
CNT15	D9 IO_L8P_T1_16
CNT16	D8 IO_L8N_T1_16
CNT17	A9 IO_L9P_T1_DQS_16
CNT18	A8 IO_L9N_T1_DQS_16
CNT19	C9 IO_L10P_T1_16
CNT20	B9 IO_L10N_T1_16
CNT21	G11 IO_L11P_T1_SRCC_16
CNT22	F10 IO_L11N_T1_SRCC_16
CNT23	E10 IO_L12P_T1_MRCC_16
CNT24	D10 IO_L12N_T1_MRCC_16
CNT25	C12 IO_L13P_T2_MRCC_16
CNT26	C11 IO_L13N_T2_MRCC_16
CNT27	E11 IO_L14P_T2_SRCC_16
CNT28	D11 IO_L14N_T2_SRCC_16
CNT29	F14 IO_L15P_T2_DQS_16
CNT30	F13 IO_L15N_T2_DQS_16
CNT31	G12 IO_L16P_T2_16
CNT32	F12 IO_L16N_T2_16
CNT33	D14 IO_L17P_T2_16
CNT34	D13 IO_L17N_T2_16
CNT35	E13 IO_L18P_T2_16
CNT36	E12 IO_L18N_T2_16
CNT37	C14 IO_L19P_T3_16
CNT38	C13 IO_L19N_T3_VREF_16
CNT39	B12 IO_L20P_T3_16
CNT40	B11 IO_L20N_T3_16
CNT41	B14 IO_L21P_T3_DQS_16
CNT42	A14 IO_L21N_T3_DQS_16
CNT43	B10 IO_L22P_T3_16
CNT44	A10 IO_L22N_T3_16
CNT45	B15 IO_L23P_T3_16
CNT46	A15 IO_L23N_T3_16
CNT47	A13 IO_L24P_T3_16
CNT48	A12 IO_L24N_T3_16
CNT49	J14 IO_25_16



U23-3	
CNT50	N16 IO_0_13
CNT51	K25 IO_L1P_T0_13
CNT52	K26 IO_L1N_T0_13
CNT53	R26 IO_L2P_T0_13
CNT54	P26 IO_L2N_T0_13
CNT55	M25 IO_L3P_T0_DQS_13
CNT56	L25 IO_L3N_T0_DQS_13
CNT57	P24 IO_L4P_T0_13
CNT58	N24 IO_L4N_T0_13
CNT59	N26 IO_L5P_T0_13
CNT60	M26 IO_L5N_T0_13
CNT61	R25 IO_L6P_T0_13
CNT62	P25 IO_L6N_T0_VREF_13
CNT63	N19 IO_L7P_T1_13
CNT64	M20 IO_L7N_T1_13
CNT65	M24 IO_L8P_T1_13
CNT66	L24 IO_L8N_T1_13
CNT67	P19 IO_L9P_T1_DQS_13
CNT68	P20 IO_L9N_T1_DQS_13
CNT69	M21 IO_L10P_T1_13
CNT70	M22 IO_L10N_T1_13
CNT71	P23 IO_L11P_T1_SRCC_13
CNT72	N23 IO_L11N_T1_SRCC_13
CNT73	N21 IO_L12P_T1_MRCC_13
CNT74	N22 IO_L12N_T1_MRCC_13
CNT75	R21 IO_L13P_T2_MRCC_13
CNT76	P21 IO_L13N_T2_MRCC_13
CNT77	R22 IO_L14P_T2_SRCC_13
CNT78	R23 IO_L14N_T2_SRCC_13
CNT79	T24 IO_L15P_T2_DQS_13
CNT80	T25 IO_L15N_T2_DQS_13
CNT81	T20 IO_L16P_T2_13
CNT82	R20 IO_L16N_T2_13
CNT83	T22 IO_L17P_T2_13
CNT84	T23 IO_L17N_T2_13
CNT85	U19 IO_L18P_T2_13
CNT86	U20 IO_L18N_T2_13
CNT87	T18 IO_L19P_T3_13
CNT88	T19 IO_L19N_T3_VREF_13
CNT89	P16 IO_L20P_T3_13
CNT90	N17 IO_L20N_T3_13
CNT91	R16 IO_L21P_T3_DQS_13
CNT92	R17 IO_L21N_T3_DQS_13
CNT93	N18 IO_L22P_T3_13
CNT94	M19 IO_L22N_T3_13
CNT95	U17 IO_L23P_T3_13
CNT96	T17 IO_L23N_T3_13
CNT97	R18 IO_L24P_T3_13
CNT98	P18 IO_L24N_T3_13
CNT99	U16 IO_25_13



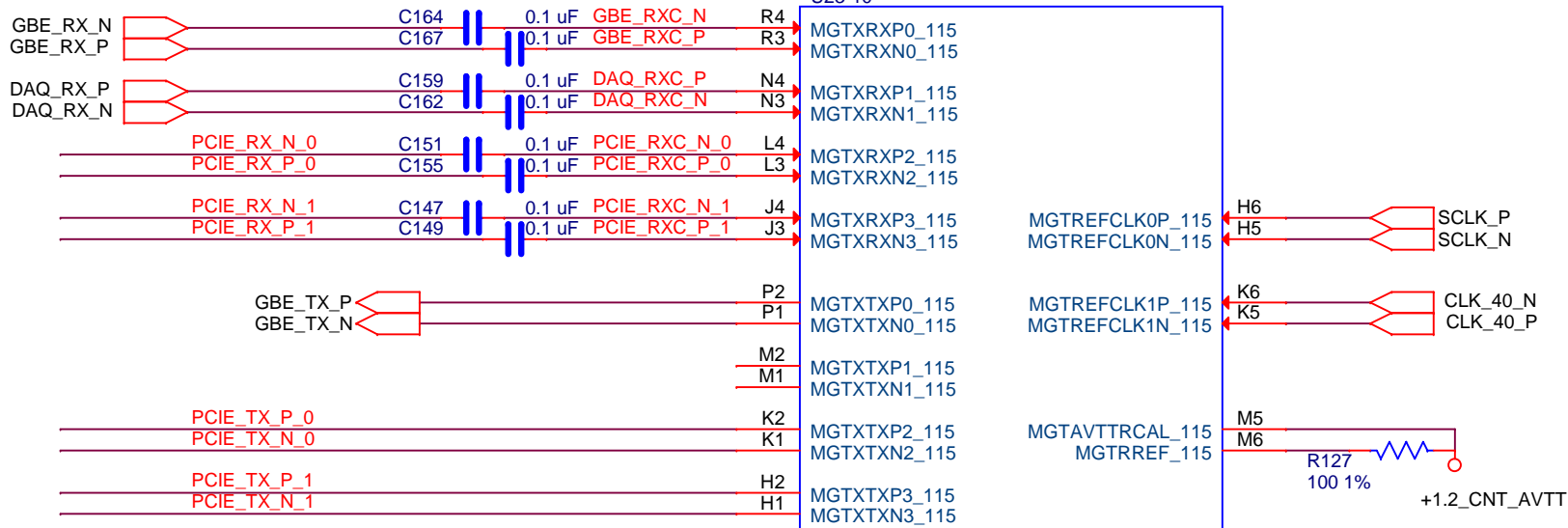
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PCIE_RX_N_[1:0]

PCIE_TX_P_[1:0]
PCIE_TX_N_[1:0]

PCIE_RXC_P_[1:0]
PCIE_RXC_N_[1:0]



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Page Modify Date = Monday, December 15, 2014
Page Number = 7

Page Size = A
RevCode =

U23-2

U21	IO_0_12
U22	IO_L1P_T0_12
V22	IO_L1N_T0_12
U24	IO_L2P_T0_12
U25	IO_L2N_T0_12
V23	IO_L3P_T0_DQS_12
V24	IO_L3N_T0_DQS_12
U26	IO_L4P_T0_12
V26	IO_L4N_T0_12
W25	IO_L5P_T0_12
W26	IO_L5N_T0_12
V21	IO_L6P_T0_12
W21	IO_L6N_T0_VREF_12
AA25	IO_L7P_T1_12
AB25	IO_L7N_T1_12
W23	IO_L8P_T1_12
W24	IO_L8N_T1_12
AB26	IO_L9P_T1_DQS_12
AC26	IO_L9N_T1_DQS_12
Y25	IO_L10P_T1_12
Y26	IO_L10N_T1_12
AA23	IO_L11P_T1_SRCC_12
AB24	IO_L11N_T1_SRCC_12
Y23	IO_L12P_T1_MRCC_12
AA24	IO_L12N_T1_MRCC_12
Y22	IO_L13P_T2_MRCC_12
AA22	IO_L13N_T2_MRCC_12
AC23	IO_L14P_T2_SRCC_12
AC24	IO_L14N_T2_SRCC_12
W20	IO_L15P_T2_DQS_12
Y21	IO_L15N_T2_DQS_12
AD23	IO_L16P_T2_12
AD24	IO_L16N_T2_12
AB22	IO_L17P_T2_12
AC22	IO_L17N_T2_12
AB21	IO_L18P_T2_12
AC21	IO_L18N_T2_12
AD21	IO_L19P_T3_12
AE21	IO_L19N_T3_VREF_12
AF24	IO_L20P_T3_12
AF25	IO_L20N_T3_12
AD26	IO_L21P_T3_DQS_12
AE26	IO_L21N_T3_DQS_12
AE23	IO_L22P_T3_12
AF23	IO_L22N_T3_12
AD25	IO_L23P_T3_12
AE25	IO_L23N_T3_12
AE22	IO_L24P_T3_12
AF22	IO_L24N_T3_12
Y20	IO_25_12
AA21	VCCO_12
AC25	VCCO_12
AD22	VCCO_12
AF26	VCCO_12
U23	VCCO_12
V20	VCCO_12
Y24	VCCO_12

+1.8V_FLASH

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U23-7

V13	IO_0_VRN_32
AE17	IO_L1P_T0_32
AF17	IO_L1N_T0_32
AF14	IO_L2P_T0_32
AF15	IO_L2N_T0_32
AE18	IO_L3P_T0_DQS_32
AF18	IO_L3N_T0_DQS_32
AD15	IO_L4P_T0_32
AE15	IO_L4N_T0_32
AF19	IO_L5P_T0_32
AF20	IO_L5N_T0_32
AD16	IO_L6P_T0_32
AE16	IO_L6N_T0_VREF_32
AA14	IO_L7P_T1_32
AA15	IO_L7N_T1_32
AC14	IO_L8P_T1_32
AD14	IO_L8N_T1_32
Y15	IO_L9P_T1_DQS_32
Y16	IO_L9N_T1_DQS_32
AB14	IO_L10P_T1_32
AB15	IO_L10N_T1_32
AA17	IO_L11P_T1_SRCC_32
AA18	IO_L11N_T1_SRCC_32
AB16	IO_L12P_T1_MRCC_32
AC16	IO_L12N_T1_MRCC_32
AC18	IO_L13P_T2_MRCC_32
AD18	IO_L13N_T2_MRCC_32
AB17	IO_L14P_T2_SRCC_32
AC17	IO_L14N_T2_SRCC_32
AD20	IO_L15P_T2_DQS_32
AE20	IO_L15N_T2_DQS_32
AA19	IO_L16P_T2_32
AA20	IO_L16N_T2_32
AC19	IO_L17P_T2_32
AD19	IO_L17N_T2_32
AB19	IO_L18P_T2_32
AB20	IO_L18N_T2_32
Y17	IO_L19P_T3_32
Y18	IO_L19N_T3_VREF_32
V16	IO_L20P_T3_32
V17	IO_L20N_T3_32
W18	IO_L21P_T3_DQS_32
W19	IO_L21N_T3_DQS_32
W15	IO_L22P_T3_32
W16	IO_L22N_T3_32
V18	IO_L23P_T3_32
V19	IO_L23N_T3_32
V14	IO_L24P_T3_32
W14	IO_L24N_T3_32
W13	IO_25_VRP_32
AB18	VCCO_32
AC15	VCCO_32
AE19	VCCO_32
AF16	VCCO_32
W17	VCCO_32
Y14	VCCO_32

+1.8V_FLASH

XC7K160T-FFG676

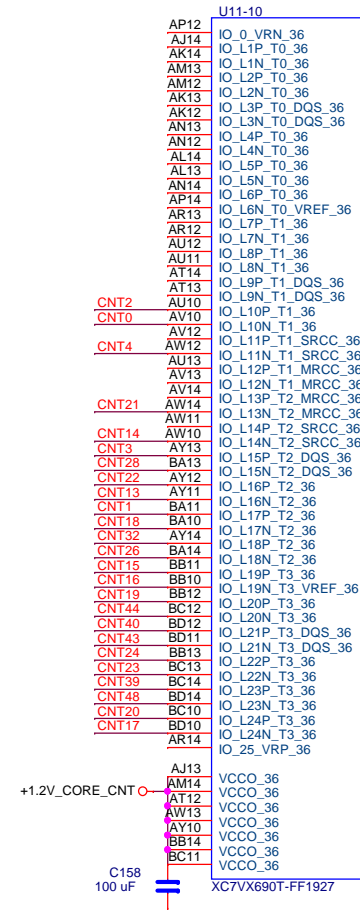
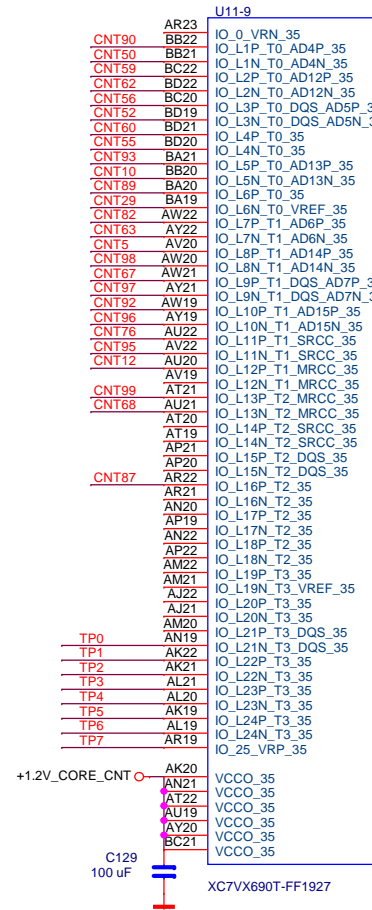
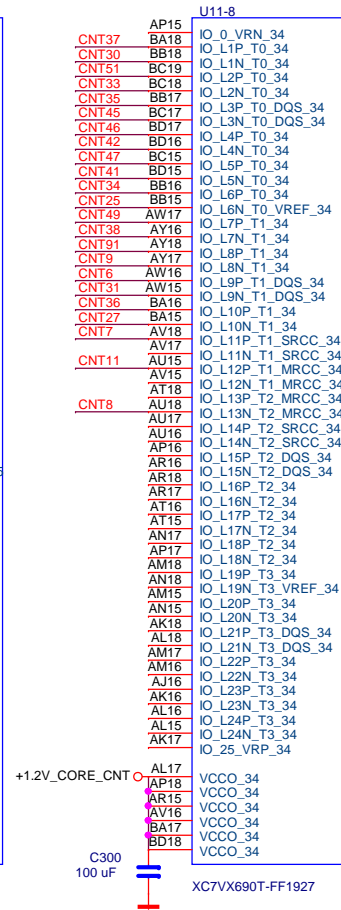
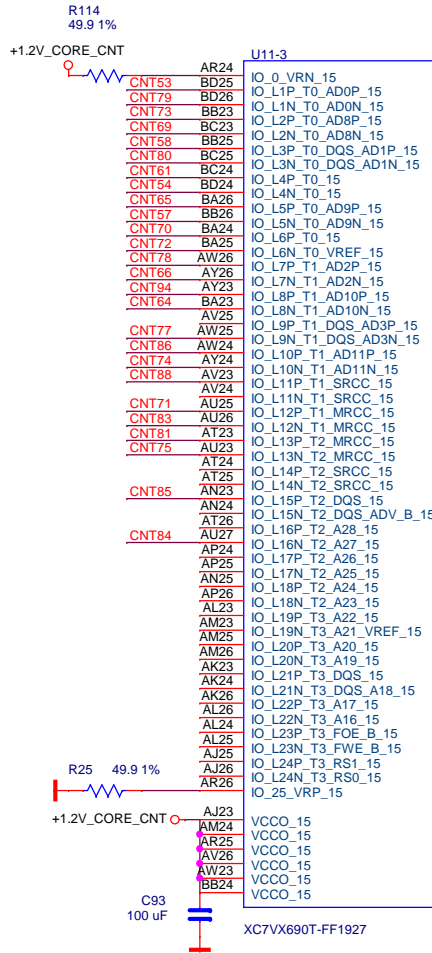
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CNT[99:0]

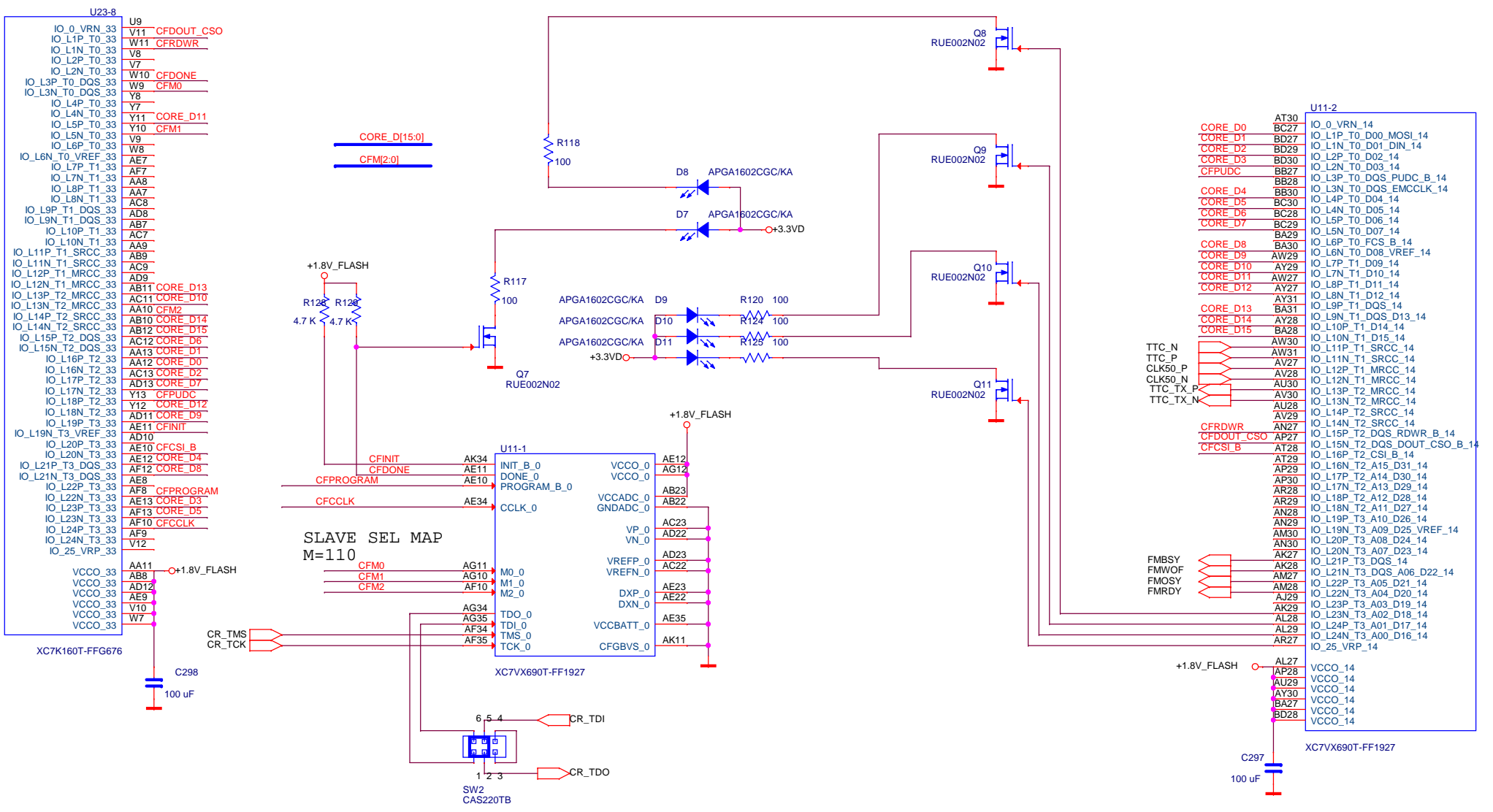
University of Florida/Physics

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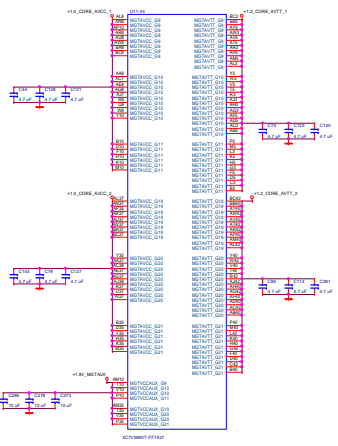
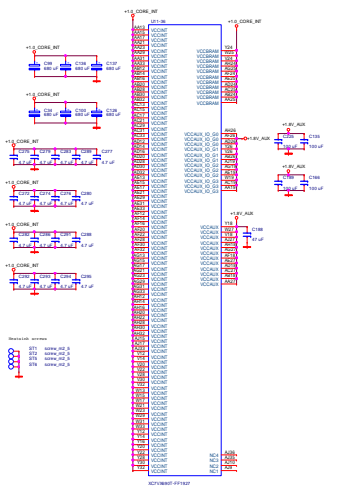
U23-6

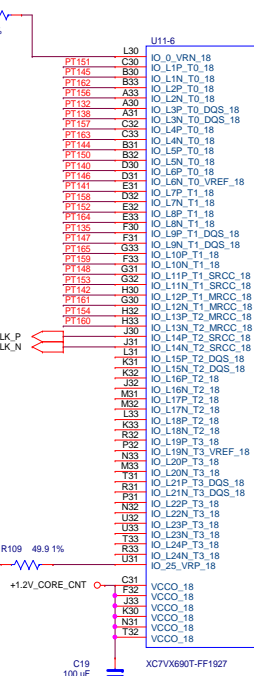
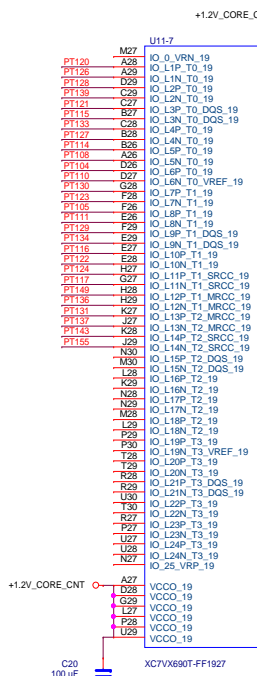
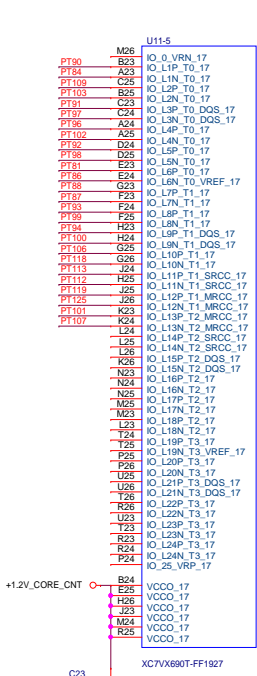
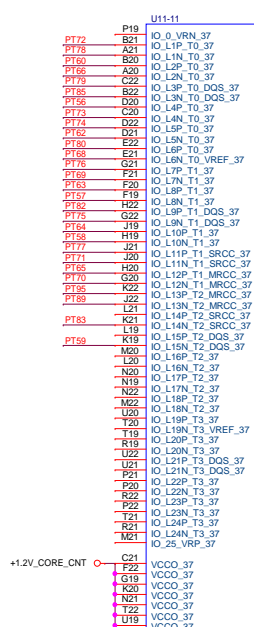
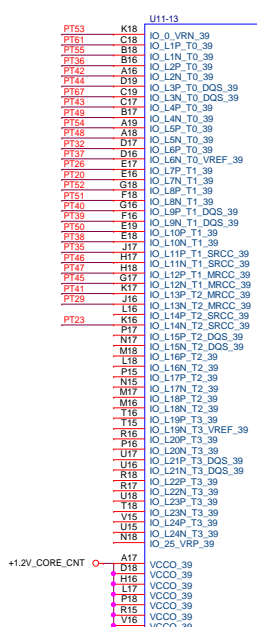
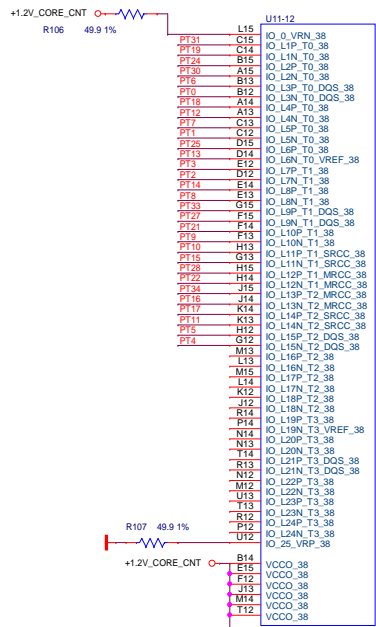
IO_0_VRN_33	V11	CFDOUT_CSO
IO_L1P_T0_33	W11	CFRDWR
IO_L1N_T0_33	V8	
IO_L2P_T0_33	V7	
IO_L2N_T0_33	W10	CFDONE
IO_L3P_T0_DQS_33	W9	CFM0
IO_L3N_T0_DQS_33	Y8	
IO_L4P_T0_33	Y7	
IO_L4N_T0_33	Y11	CORE_D11
IO_L5P_T0_33	Y10	CFM1
IO_L5N_T0_33	V9	
IO_L6P_T0_33	W8	
IO_L6N_T0_VREF_33	AE7	
IO_L7P_T1_33	AF7	
IO_L7N_T1_33	AA8	
IO_L8P_T1_33	AA7	
IO_L8N_T1_33	AC8	
IO_L9P_T1_DQS_33	AD8	
IO_L9N_T1_DQS_33	AB7	
IO_L10P_T1_33	AC7	
IO_L10N_T1_33	AA9	
IO_L11P_T1_SRCC_33	AB9	
IO_L11N_T1_SRCC_33	AC9	
IO_L12P_T1_MRCC_33	AD9	
IO_L12N_T1_MRCC_33	AB11	CORE_D13
IO_L13P_T2_MRCC_33	AC11	CORE_D10
IO_L13N_T2_MRCC_33	AA10	CFM2
IO_L14P_T2_SRCC_33	AB10	CORE_D14
IO_L14N_T2_SRCC_33	AB12	CORE_D15
IO_L15P_T2_DQS_33	AC12	CORE_D6
IO_L15N_T2_DQS_33	AD13	CORE_D7
IO_L16P_T2_33	AA13	CORE_D1
IO_L16N_T2_33	AA12	CORE_D0
IO_L17P_T2_33	AC13	CORE_D2
IO_L17N_T2_33	AD13	CORE_D7
IO_L18P_T2_33	Y13	CFPUDC
IO_L18N_T2_33	Y12	CORE_D12
IO_L19P_T3_33	AD11	CORE_D9
IO_L19N_T3_VREF_33	AE11	CFINIT
IO_L20P_T3_33	AD10	
IO_L20N_T3_33	AE10	CFCSI_B
IO_L21P_T3_DQS_33	AF12	CORE_D4
IO_L21N_T3_DQS_33	AE8	
IO_L22P_T3_33	AF8	CFPROGRAM
IO_L22N_T3_33	AE13	CORE_D3
IO_L23P_T3_33	AF13	CORE_D5
IO_L23N_T3_33	AF10	CFCLK
IO_L24P_T3_33	AF9	
IO_L24N_T3_33	V12	
IO_25_VRP_33	AA11	
VCCO_33	AB8	
VCCO_33	AD12	
VCCO_33	AE9	
VCCO_33	V10	
VCCO_33	W7	

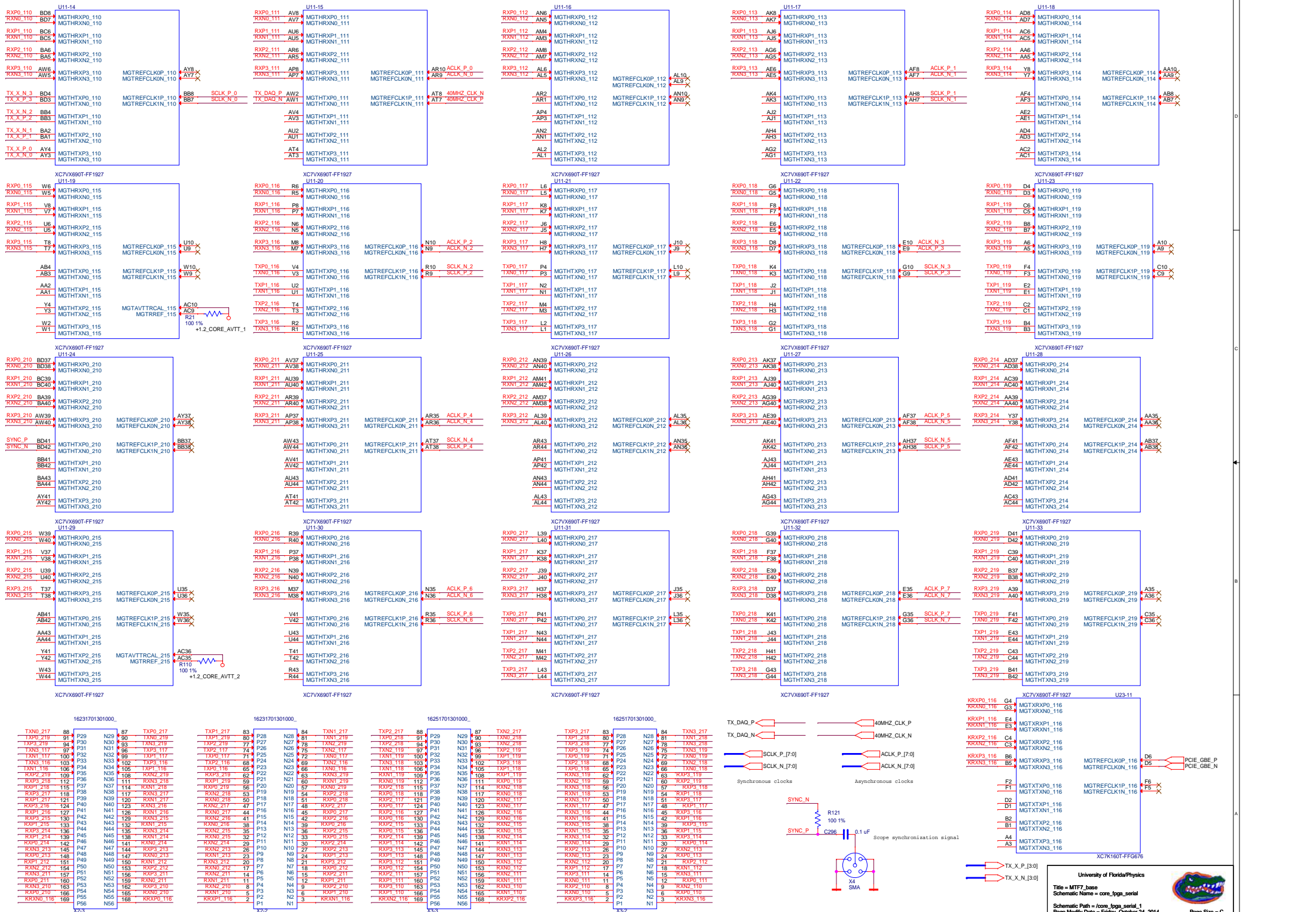
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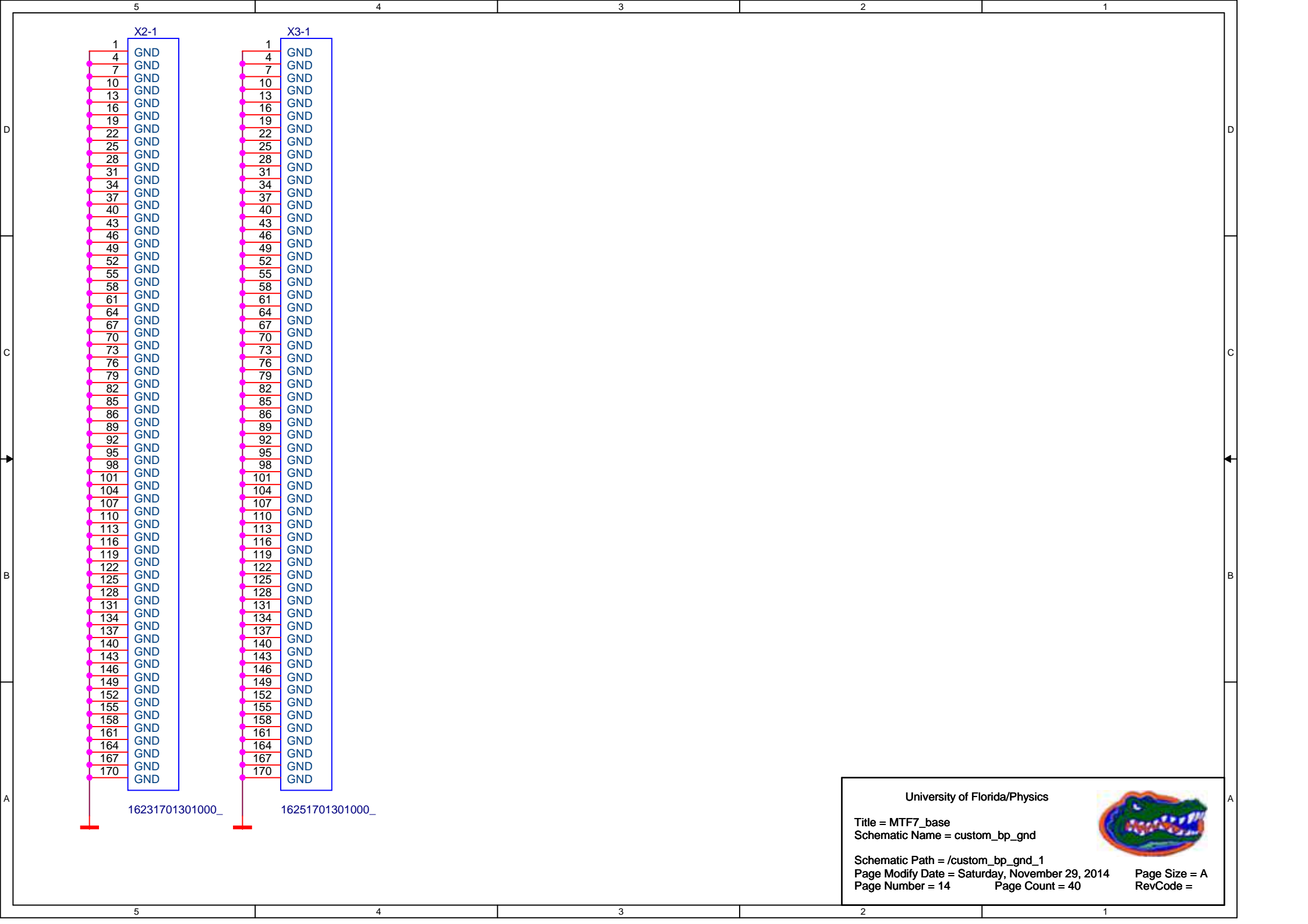
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CORE_D1	BD27	IO_L1P_T0_D00_MOSI_14
CORE_D2	BD29	IO_L1N_T0_D01_DIN_14
CORE_D3	BD30	IO_L2P_T0_D02_14
CFPUDC	BB27	IO_L2N_T0_D03_14
	BB28	IO_L3P_T0_DQS_PUDC_B_14
CORE_D4	BB30	IO_L3N_T0_DQS_EMCCLK_14
CORE_D5	BC30	IO_L4P_T0_D04_14
CORE_D6	BC28	IO_L4N_T0_D05_14
CORE_D7	BC29	IO_L5P_T0_D06_14
	BC29	IO_L5N_T0_D07_14
CORE_D8	BA29	IO_L6P_T0_FCS_B_14
CORE_D9	BA30	IO_L6N_T0_D08_VREF_14
CORE_D10	AY29	IO_L7P_T1_D09_14
CORE_D11	AW27	IO_L7N_T1_D10_14
CORE_D12	AY27	IO_L8P_T1_D11_14
	AY31	IO_L8N_T1_D12_14
CORE_D13	BA31	IO_L9P_T1_DQS_14
CORE_D14	AY28	IO_L9N_T1_DQS_D13_14
CORE_D15	BA28	IO_L10P_T1_D14_14
	AW30	IO_L10N_T1_D15_14
TTC_N	AW30	IO_L11P_T1_SRCC_14
TTC_P	AW31	IO_L11N_T1_SRCC_14
CLK50_P	AV27	IO_L12P_T1_MRCC_14
CLK50_N	AV28	IO_L12N_T1_MRCC_14
TTC_TX_P	AV30	IO_L13P_T2_MRCC_14
TTC_TX_N	AV30	IO_L13N_T2_MRCC_14
	AU28	IO_L14P_T2_SRCC_14
CFRDWR	AV29	IO_L14N_T2_SRCC_14
CFDOUT_CSO	AN27	IO_L15P_T2_DQS_RDWR_B_14
CFCSI_B	AP27	IO_L15N_T2_DQS_DOUT_CSO_B_14
	AT28	IO_L16P_T2_CSI_B_14
	AT29	IO_L16N_T2_A15_D31_14
	AP29	IO_L17P_T2_A14_D30_14
	AP30	IO_L17N_T2_A13_D29_14
	AR28	IO_L18P_T2_A12_D28_14
	AR29	IO_L18N_T2_A11_D27_14
	AN28	IO_L19P_T3_A10_D26_14
	AN29	IO_L19N_T3_A09_D25_VREF_14
	AM30	IO_L20P_T3_A08_D24_14
	AN30	IO_L20N_T3_A07_D23_14
FMSBY	AK27	IO_L21P_T3_DQS_14
FMWOF	AK28	IO_L21N_T3_DQS_A06_D22_14
FMSY	AM27	IO_L22P_T3_A05_D21_14
FMRDY	AM28	IO_L22N_T3_A04_D20_14
	AJ29	IO_L23P_T3_A03_D19_14
	AK29	IO_L23N_T3_A02_D18_14
	AL28	IO_L24P_T3_A01_D17_14
	AL29	IO_L24N_T3_A00_D16_14
	AR27	IO_25_VRP_14
	AL27	VCCO_14
	AP28	VCCO_14
	AU29	VCCO_14
	AY30	VCCO_14
	BA27	VCCO_14
	BD28	VCCO_14

001 002 003 004 005 006 007 008 009 010 011 012 013 014 015 016 017 018 019 020 021 022 023 024 025 026 027 028 029 030 031 032 033 034 035 036 037 038 039 040 041 042 043 044 045 046 047 048 049 050 051 052 053 054 055 056 057 058 059 060 061 062 063 064 065 066 067 068 069 070 071 072 073 074 075 076 077 078 079 080 081 082 083 084 085 086 087 088 089 090 091 092 093 094 095 096 097 098 099 100 101 102 103 104 105 106 107 108 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 178 179 180 181 182 183 184 185 186 187 188 189 190 191 192 193 194 195 196 197 198 199 200 201 202 203 204 205 206 207 208 209 210 211 212 213 214 215 216 217 218 219 220 221 222 223 224 225 226 227 228 229 230 231 232 233 234 235 236 237 238 239 240 241 242 243 244 245 246 247 248 249 250 251 252 253 254 255 256 257 258 259 260 261 262 263 264 265 266 267 268 269 270 271 272 273 274 275 276 277 278 279 280 281 282 283 284 285 286 287 288 289 290 291 292 293 294 295 296 297 298 299 300 301 302 303 304 305 306 307 308 309 310 311 312 313 314 315 316 317 318 319 320 321 322 323 324 325 326 327 328 329 330 331 332 333 334 335 336 337 338 339 340 341 342 343 344 345 346 347 348 349 350 351 352 353 354 355 356 357 358 359 360 361 362 363 364 365 366 367 368 369 370 371 372 373 374 375 376 377 378 379 380 381 382 383 384 385 386 387 388 389 390 391 392 393 394 395 396 397 398 399 400 401 402 403 404 405 406 407 408 409 410 411 412 413 414 415 416 417 418 419 420 421 422 423 424 425 426 427 428 429 430 431 432 433 434 435 436 437 438 439 440 441 442 443 444 445 446 447 448 449 450 451 452 453 454 455 456 457 458 459 460 461 462 463 464 465 466 467 468 469 470 471 472 473 474 475 476 477 478 479 480 481 482 483 484 485 486 487 488 489 490 491 492 493 494 495 496 497 498 499 500 501 502 503 504 505 506 507 508 509 510 511 512 513 514 515 516 517 518 519 520 521 522 523 524 525 526 527 528 529 530 531 532 533 534 535 536 537 538 539 540 541 542 543 544 545 546 547 548 549 550 551 552 553 554 555 556 557 558 559 560 561 562 563 564 565 566 567 568 569 570 571 572 573 574 575 576 577 578 579 580 581 582 583 584 585 586 587 588 589 590 591 592 593 594 595 596 597 598 599 600 601 602 603 604 605 606 607 608 609 610 611 612 613 614 615 616 617 618 619 620 621 622 623 624 625 626 627 628 629 630 631 632 633 634 635 636 637 638 639 640 641 642 643 644 645 646 647 648 649 650 651 652 653 654 655 656 657 658 659 660 661 662 663 664 665 666 667 668 669 670 671 672 673 674 675 676 677 678 679 680 681 682 683 684 685 686 687 688 689 690 691 692 693 694 695 696 697 698 699 700 701 702 703 704 705 706 707 708 709 710 711 712 713 714 715 716 717 718 719 720 721 722 723 724 725 726 727 728 729 730 731 732 733 734 735 736 737 738 739 740 741 742 743 744 745 746 747 748 749 750 751 752 753 754 755 756 757 758 759 760 761 762 763 764 765 766 767 768 769 770 771 772 773 774 775 776 777 778 779 780 781 782 783 784 785 786 787 788 789 790 791 792 793 794 795 796 797 798 799 800 801 802 803 804 805 806 807 808 809 810 811 812 813 814 815 816 817 818 819 820 821 822 823 824 825 826 827 828 829 830 831 832 833 834 835 836 837 838 839 840 841 842 843 844 845 846 847 848 849 850 851 852 853 854 855 856 857 858 859 860 861 862 863 864 865 866 867 868 869 870 871 872 873 874 875 876 877 878 879 880 881 882 883 884 885 886 887 888 889 890 891 892 893 894 895 896 897 898 899 900 901 902 903 904 905 906 907 908 909 910 911 912 913 914 915 916 917 918 919 920 921 922 923 924 925 926 927 928 929 930 931 932 933 934 935 936 937 938 939 940 941 942 943 944 945 946 947 948 949 950 951 952 953 954 955 956 957 958 959 960 961 962 963 964 965 966 967 968 969 970 971 972 973 974 975 976 977 978 979 980 981 982 983 984 985 986 987 988 989 990 991 992 993 994 995 996 997 998 999 1000









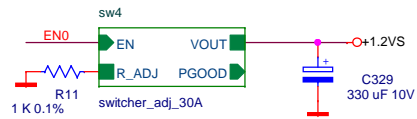
University of Florida/Physics

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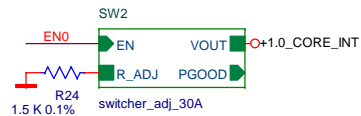


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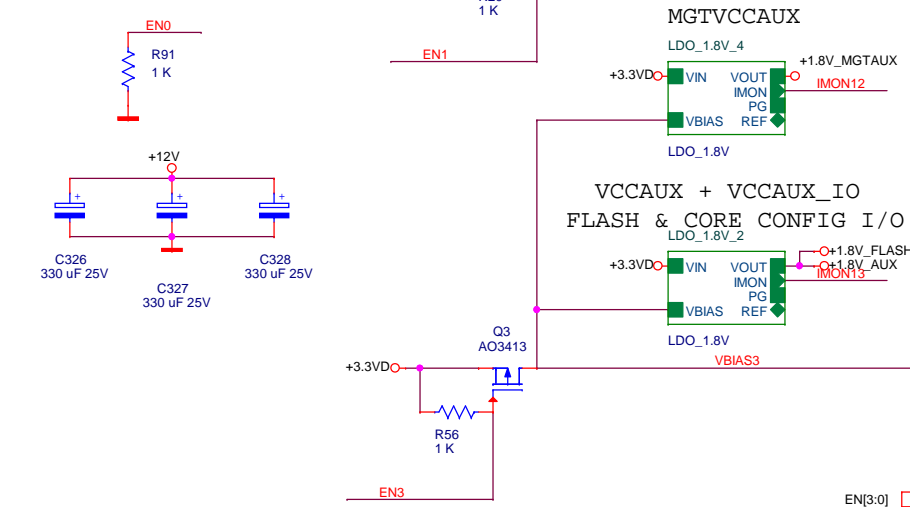
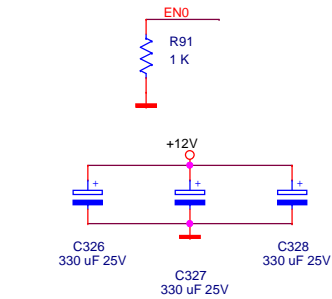
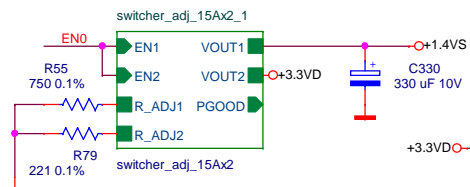
SOURCE FOR 1V LDOs



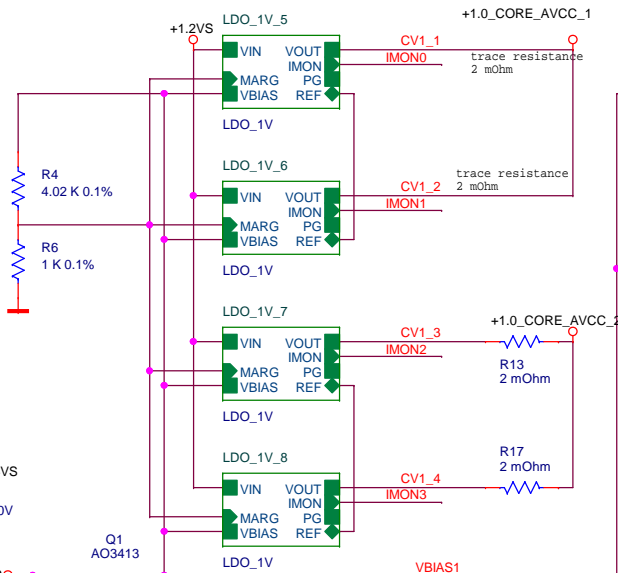
CORE VCCINT



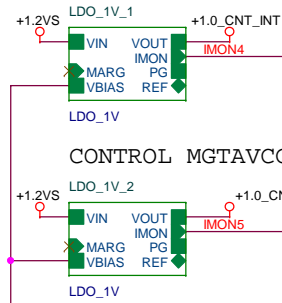
SOURCE FOR 1.2V LDOs
3.3V POWER, BIAS V FOR LDOs



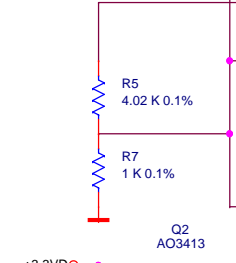
CORE MGTAVCC
Left and Right
side separated



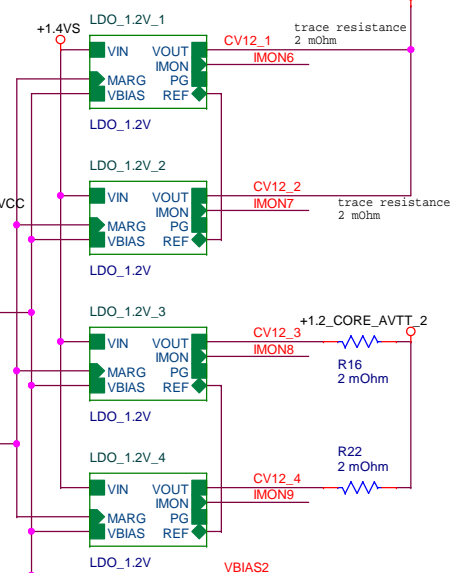
CONTROL VCCINT



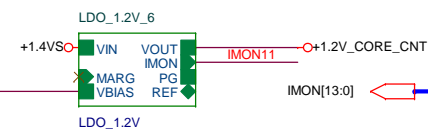
CONTROL MGTAVCC



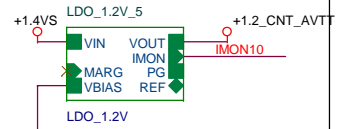
CORE MGTAVTT
Left and Right
side separated



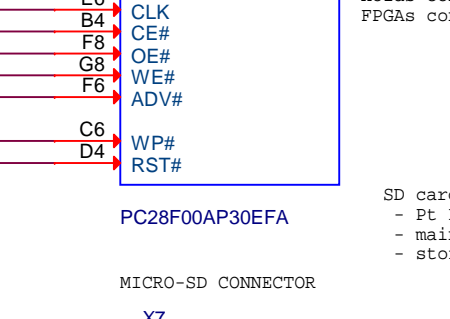
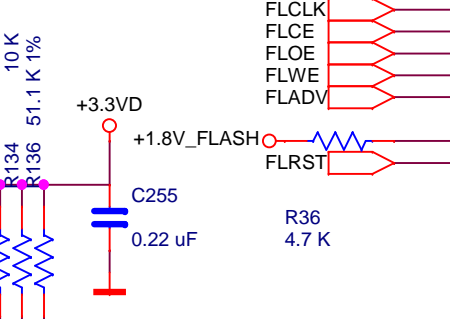
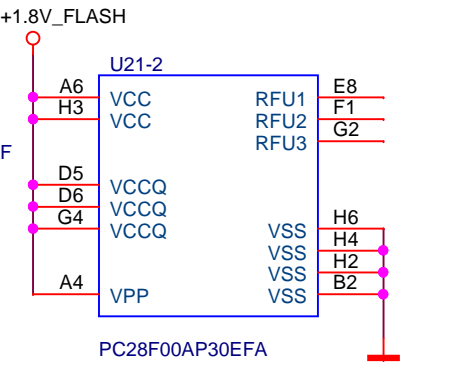
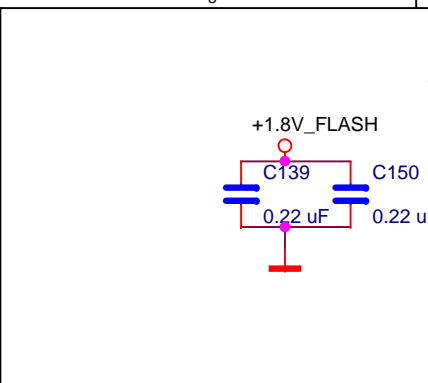
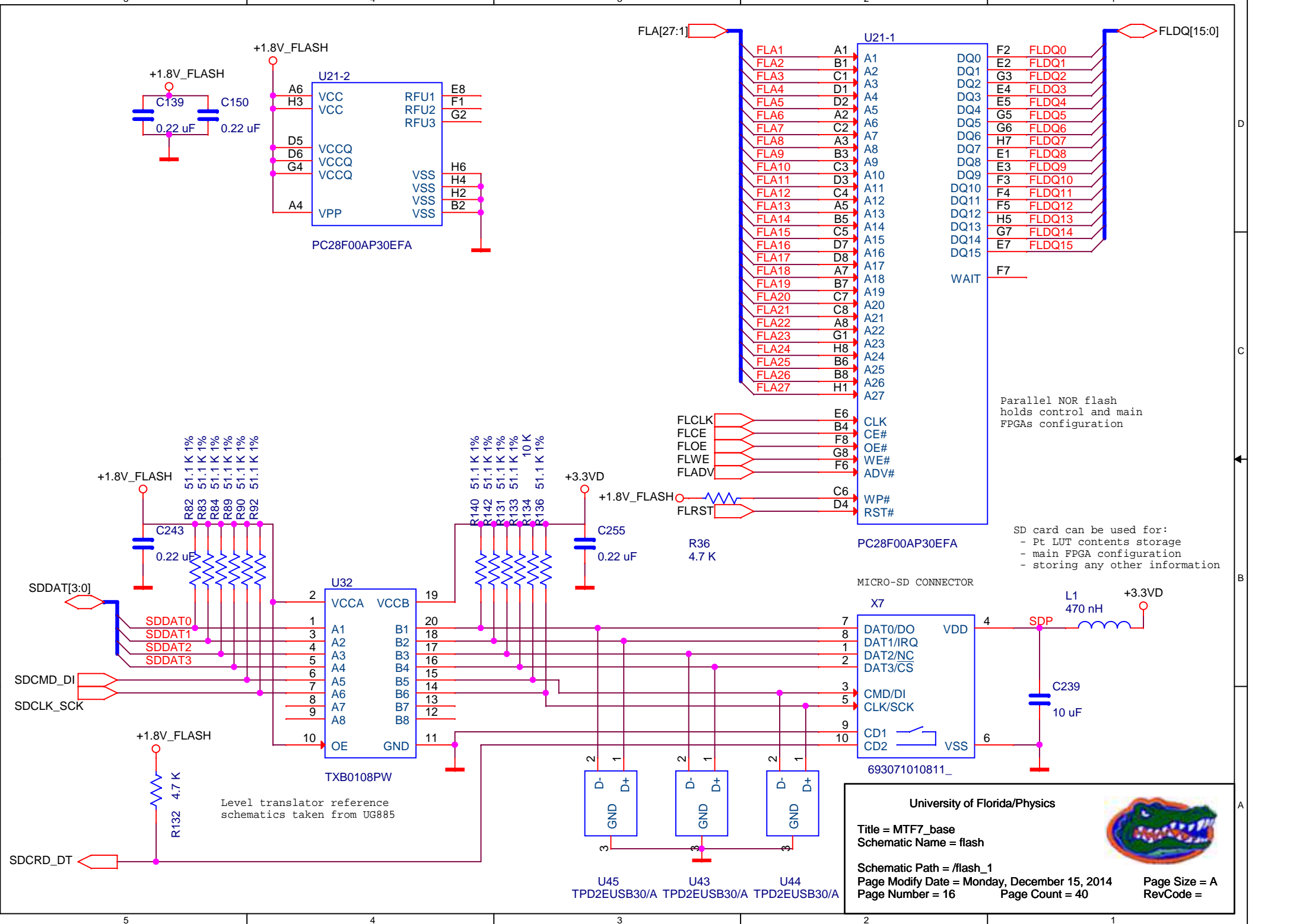
PT I/O
CORE CONTROL I/O



CONTROL MGTAVTT

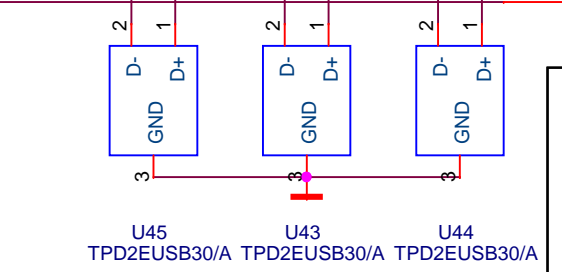
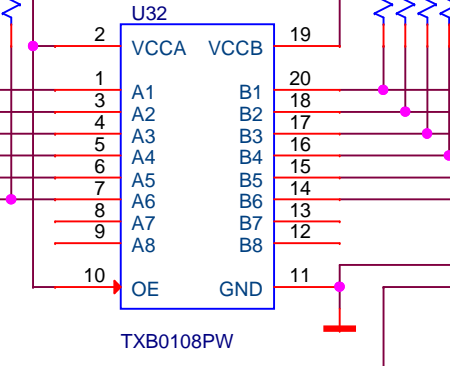
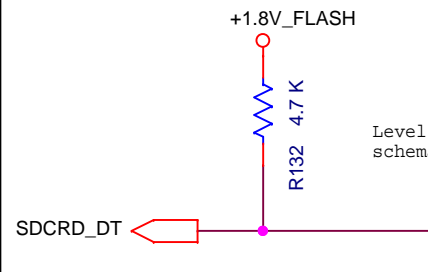


IMON0	R2	1 K 0.1%
IMON1	R8	1 K 0.1%
IMON2	R14	1 K 0.1%
IMON3	R18	1 K 0.1%
IMON4	R77	1 K 0.1%
IMON5	R80	1 K 0.1%
IMON6	R3	1 K 0.1%
IMON7	R9	1 K 0.1%
IMON8	R19	1 K 0.1%
IMON9	R23	1 K 0.1%
IMON10	R81	1 K 0.1%
IMON11	R15	1 K 0.1%
IMON12	R28	1 K 0.1%
IMON13	R35	1 K 0.1%




SD card can be used for:

- Pt LUT contents storage
- main FPGA configuration
- storing any other information



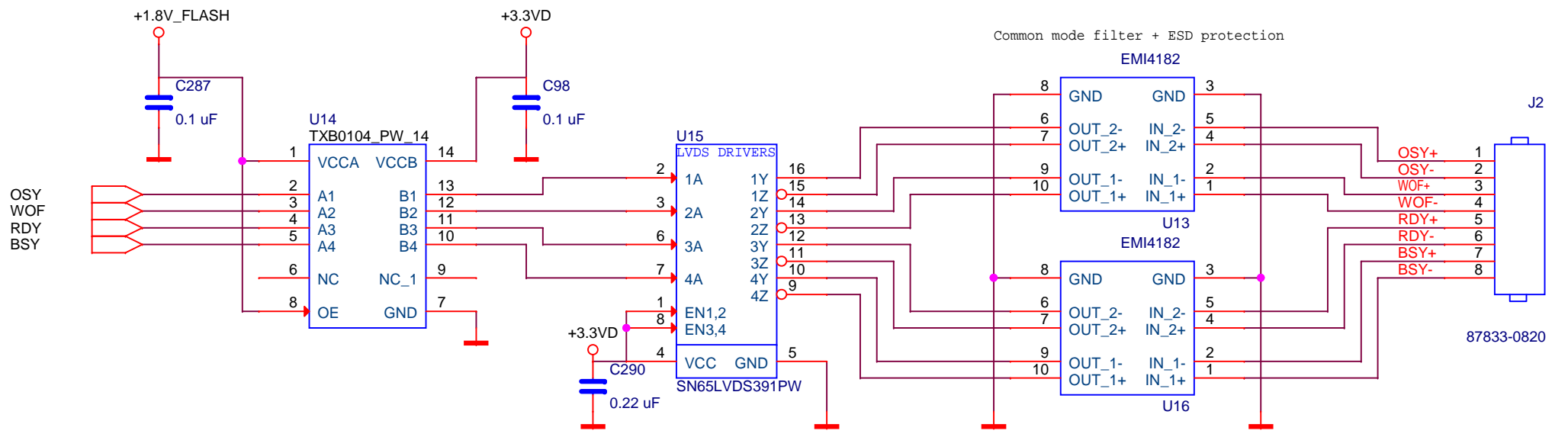
University of Florida/Physics

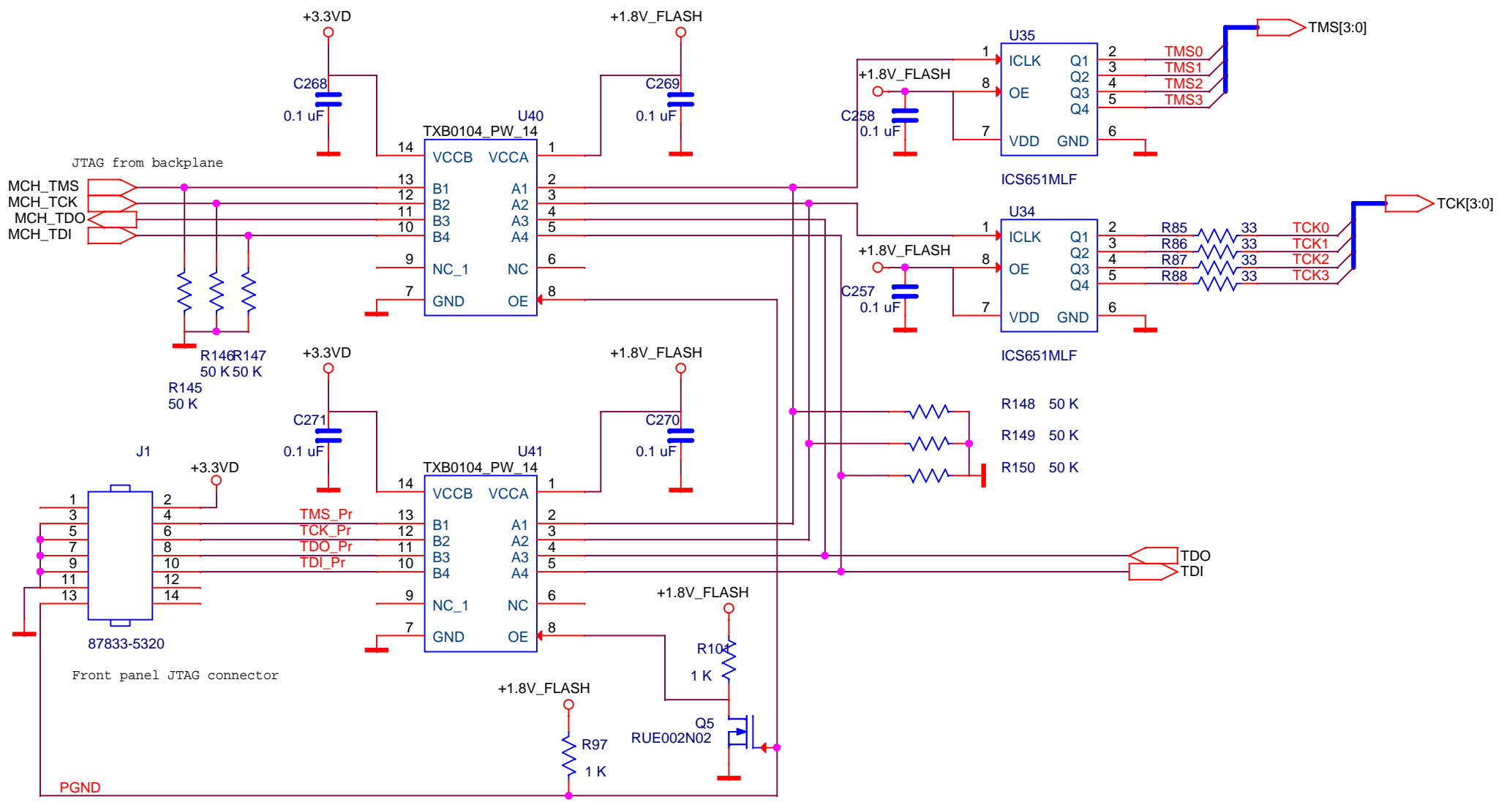


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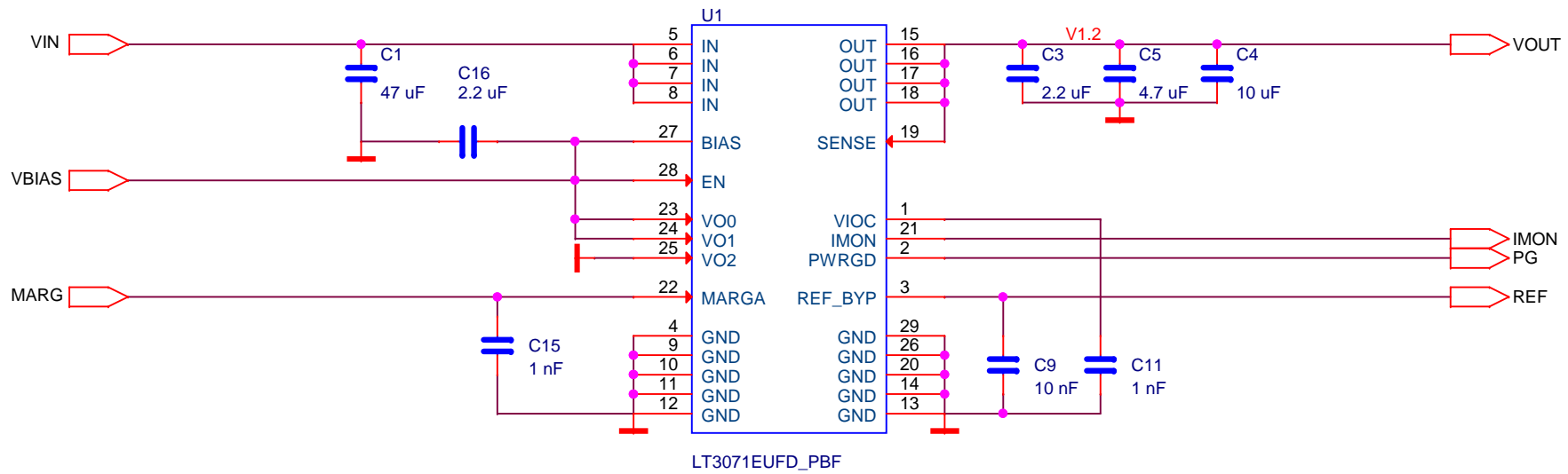
PGND is shorted to ground when cable is in use

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Schematic Name = jtag



Schematic Path = /jtag_1
Page Modify Date = Monday, October 20, 2014
Page Number = 18 Page Count = 40 Page Size = A
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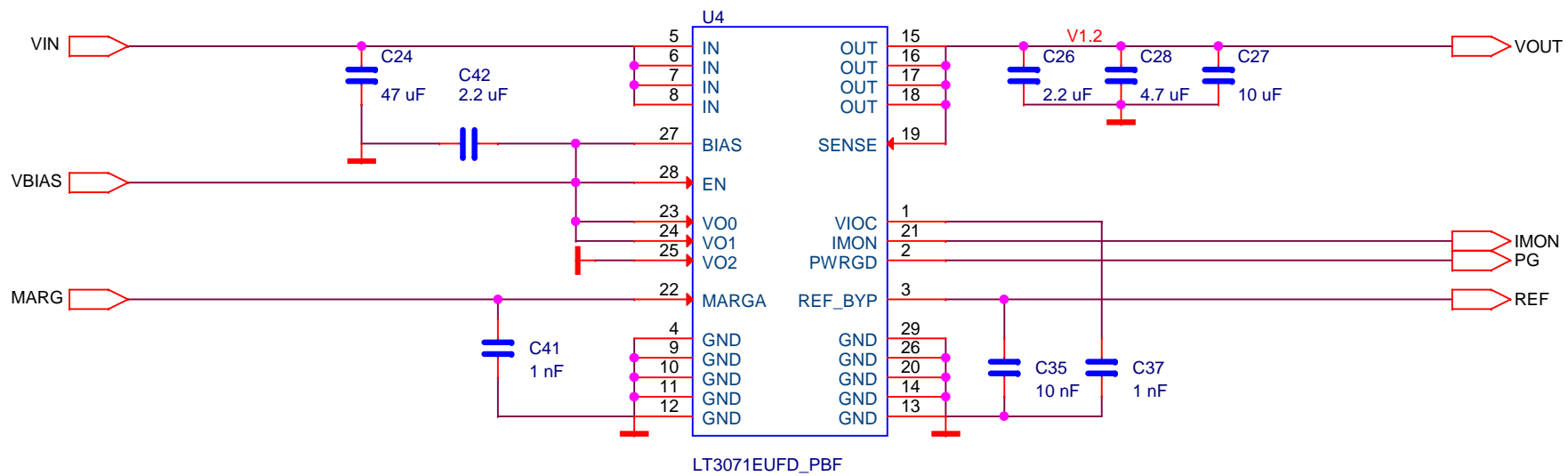
University of Florida/Physics

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Schematic Path = /dc-dc_1/LDO_1.2V_1
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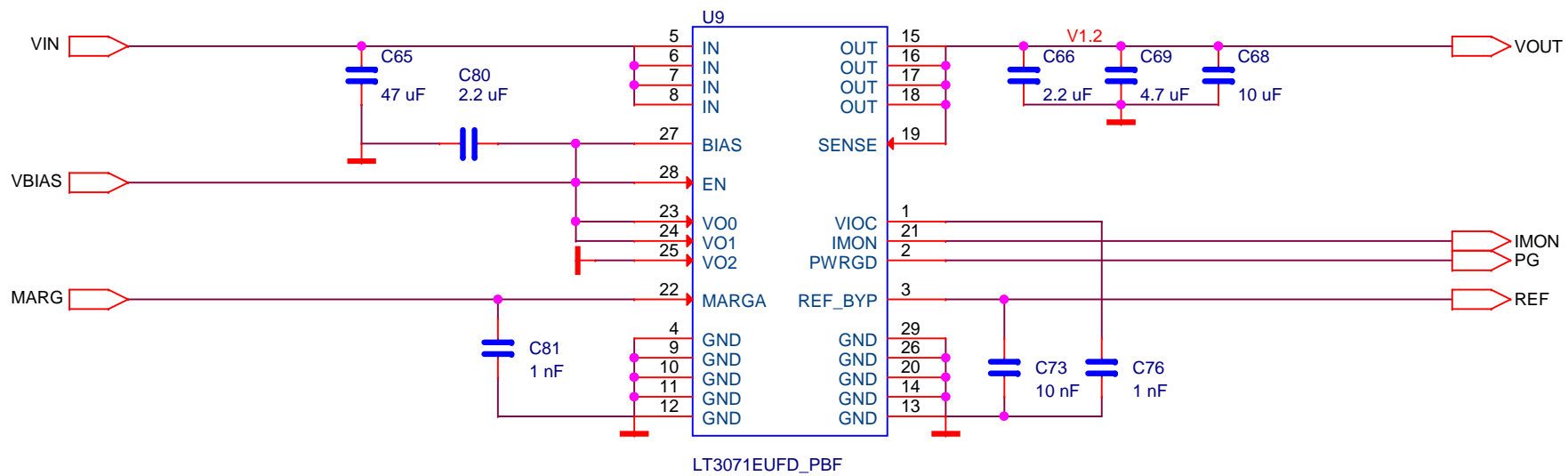
University of Florida/Physics

Title = MTF7_base
Schematic Name = LDO_1.2V



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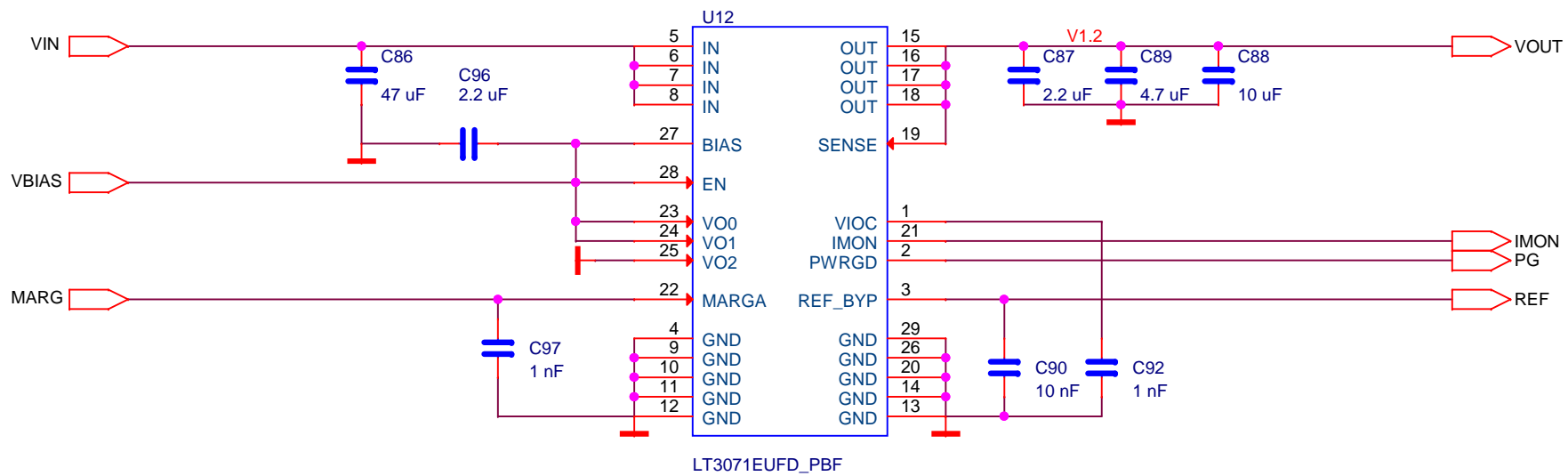
University of Florida/Physics

Title = MTF7_base
Schematic Name = LDO_1.2V



Schematic Path = /dc-dc_1/LDO_1.2V_3
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University of Florida/Physics

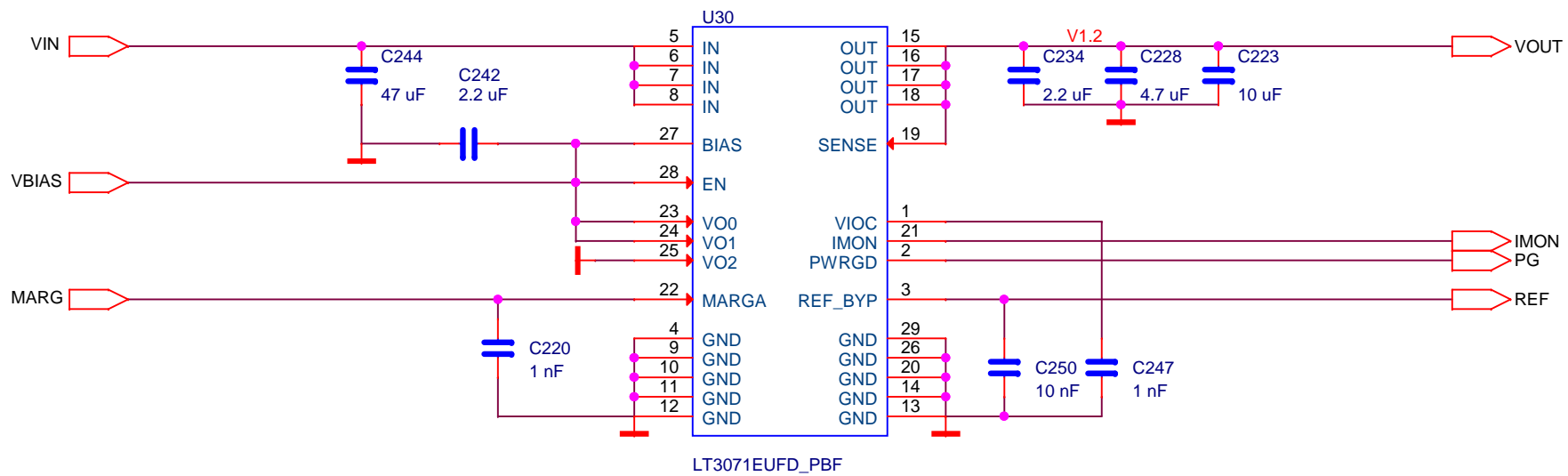
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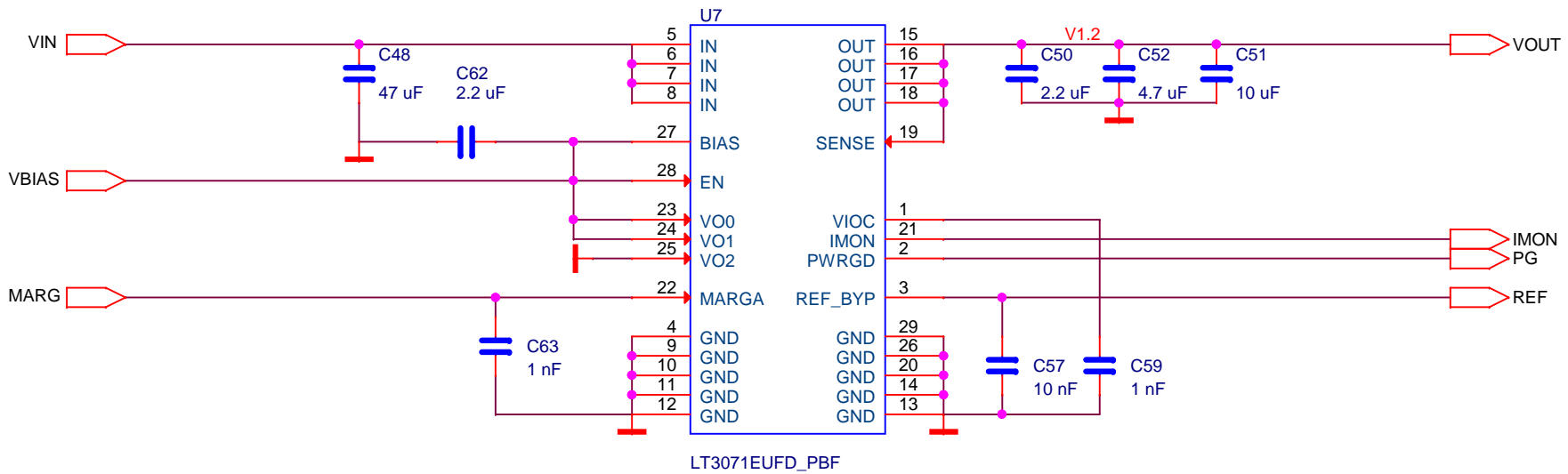
University of Florida/Physics

Title = MTF7_base
Schematic Name = LDO_1.2V



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University of Florida/Physics

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 Schematic Name = LDO_1.2V

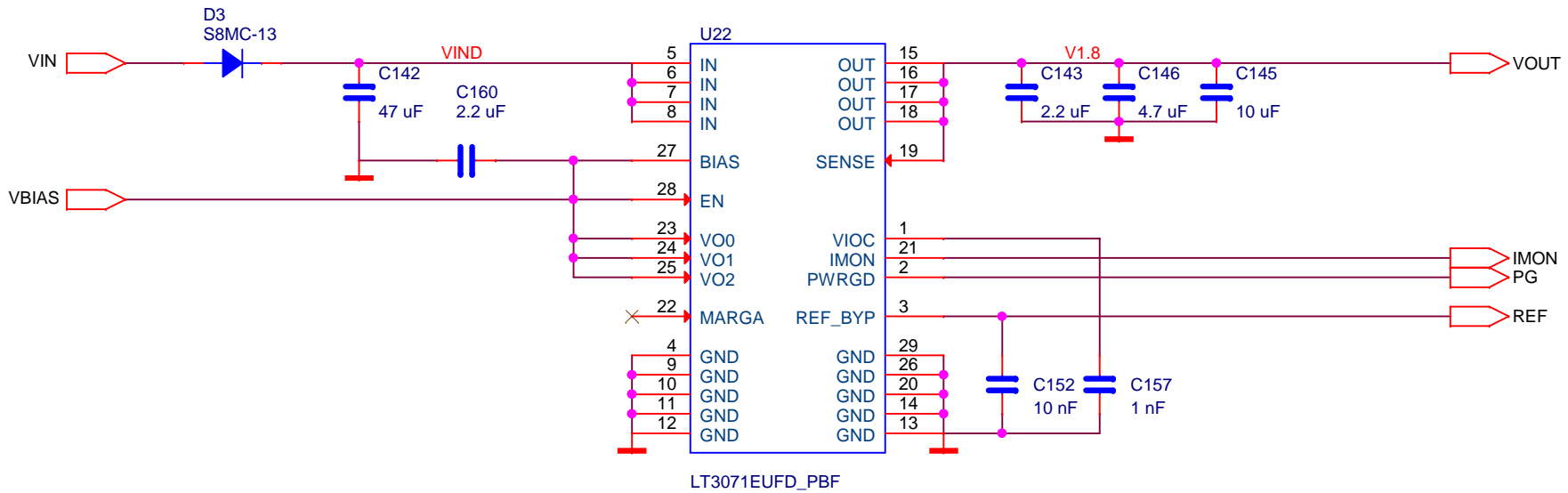


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Max VIN for LC3071 is 3.0V
 Diode is used to drop it down from 3.3V



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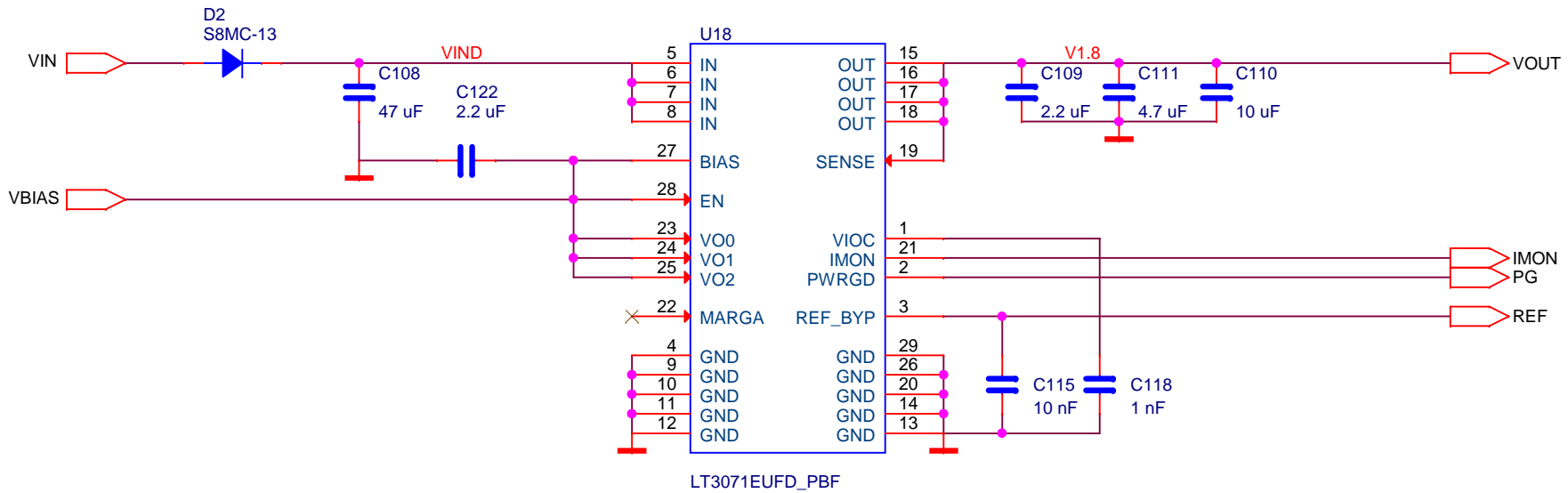
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Max VIN for LC3071 is 3.0V
 Diode is used to drop it down from 3.3V



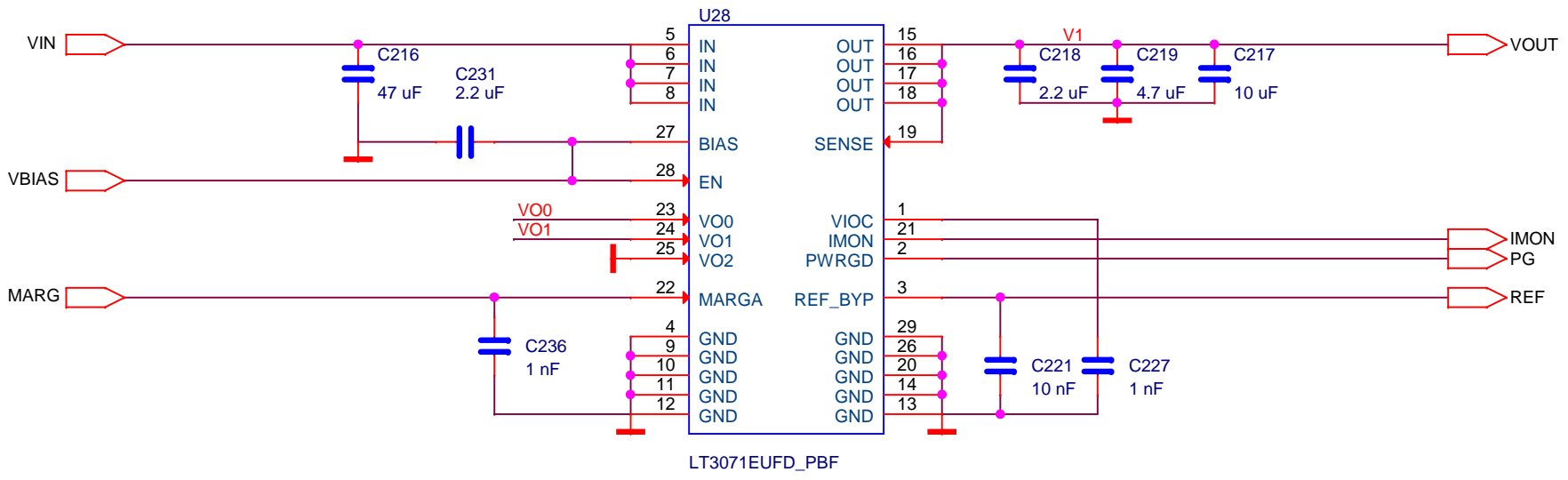
University of Florida/Physics

Title = MTF7_base
 Schematic Name = LDO_1.8V



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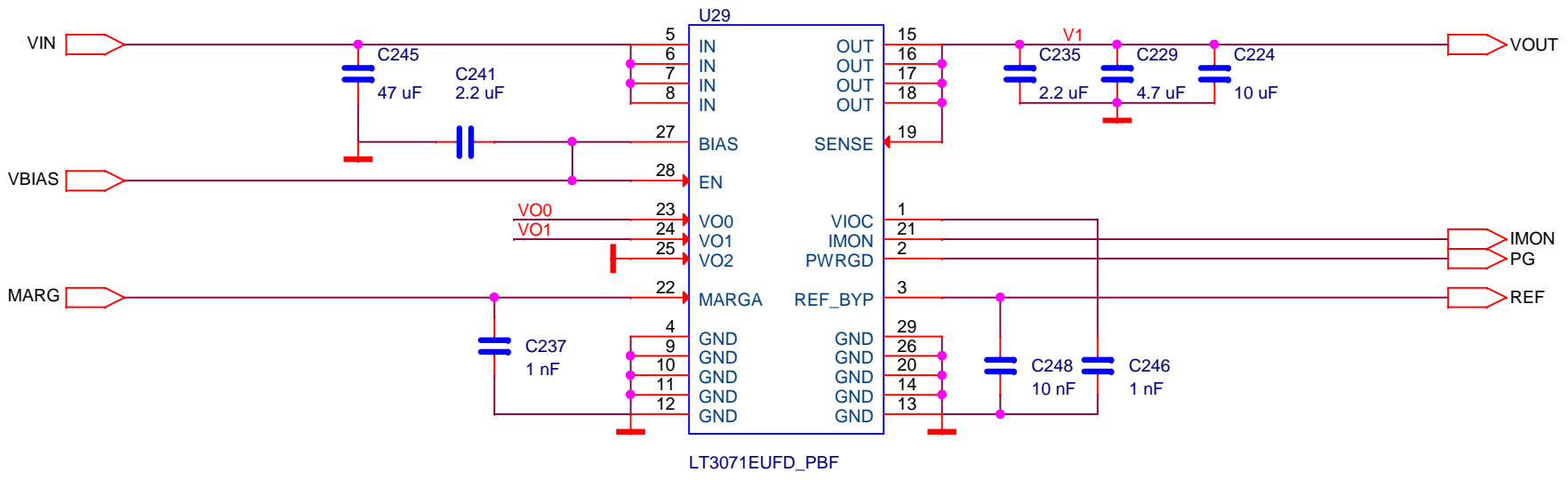
University of Florida/Physics

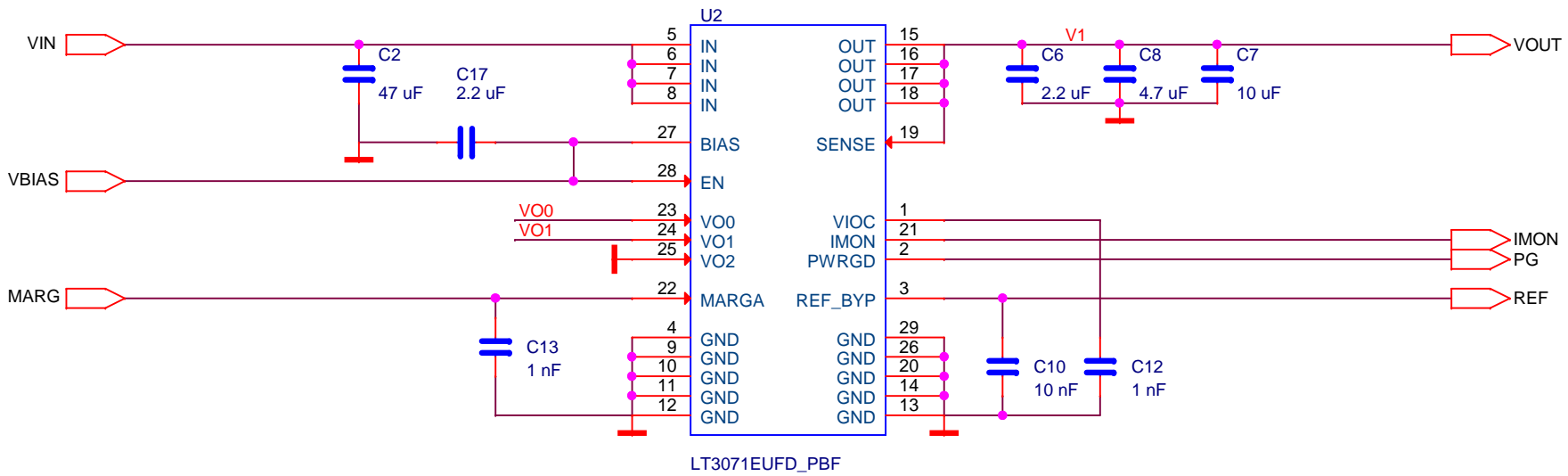
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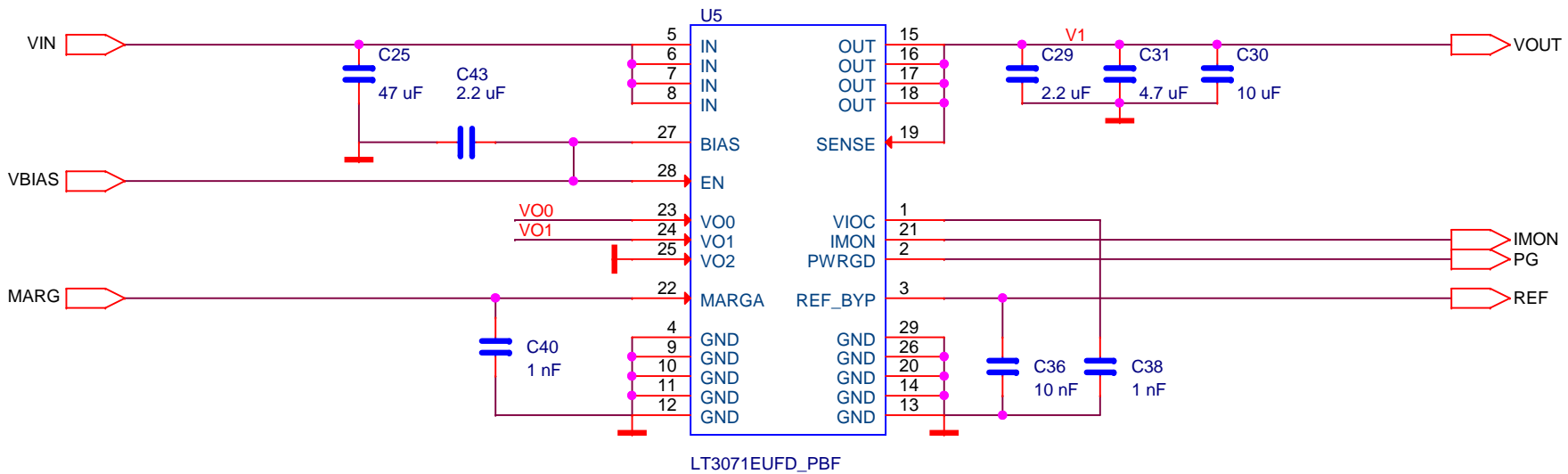
University of Florida/Physics

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Schematic Name = LDO_1V



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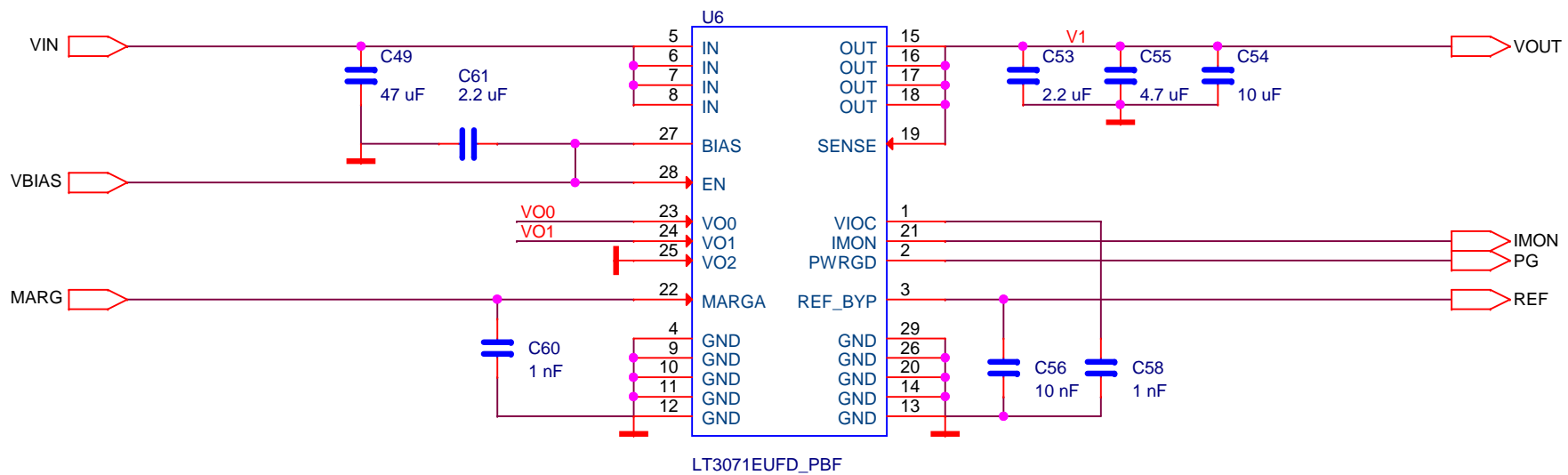
University of Florida/Physics

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Schematic Name = LDO_1V



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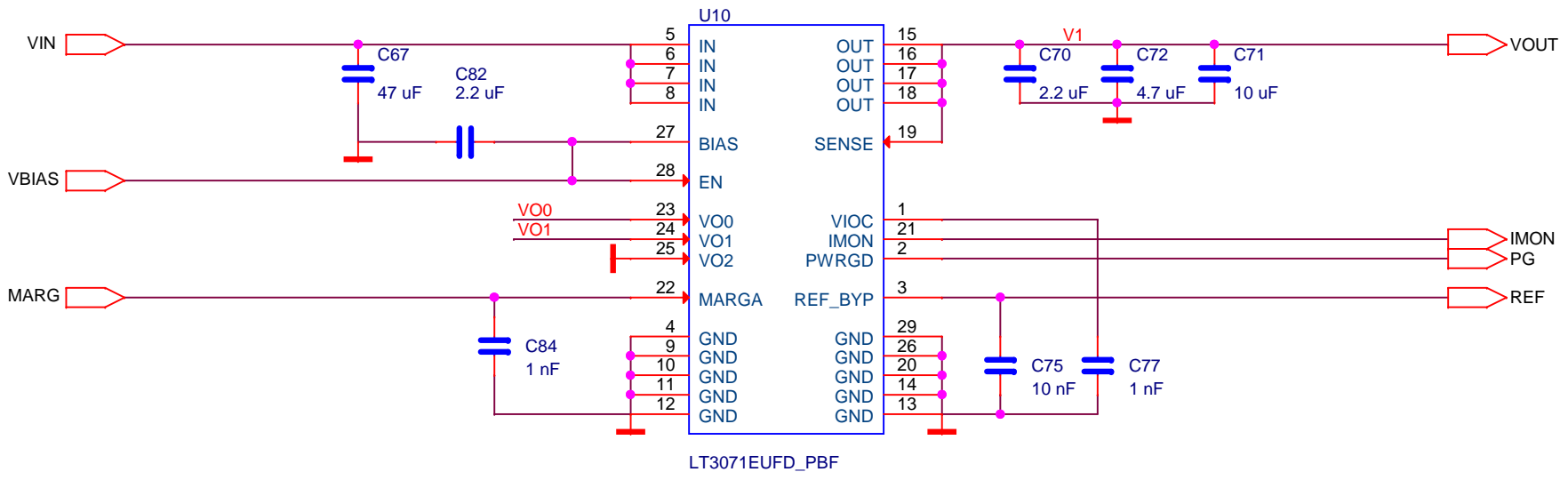
University of Florida/Physics

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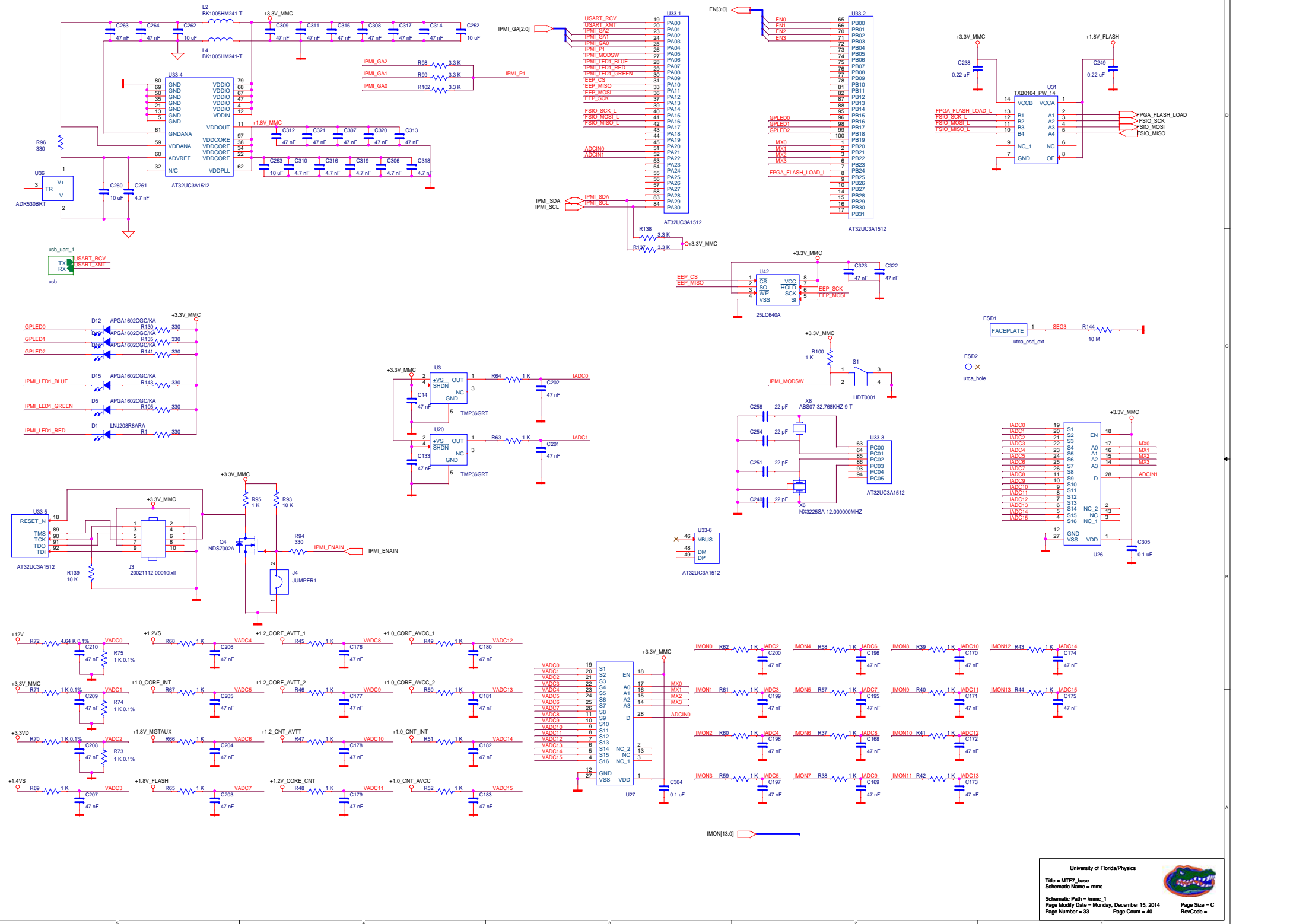


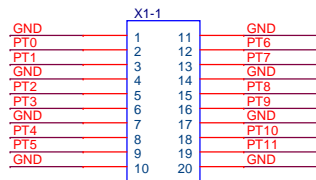
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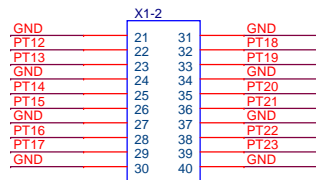


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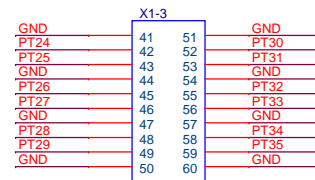




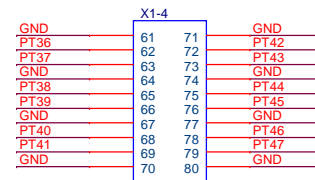
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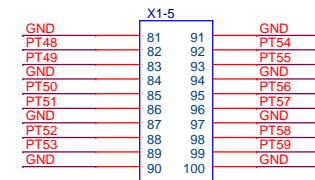
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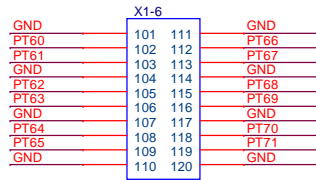
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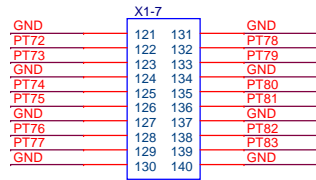
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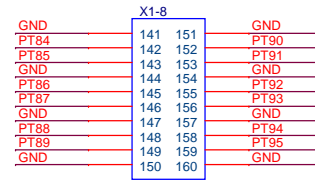
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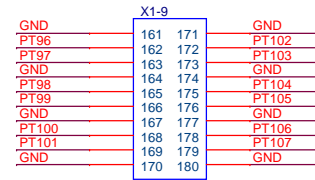
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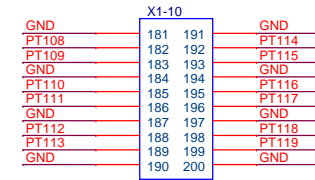
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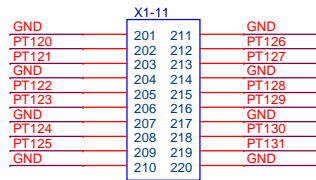
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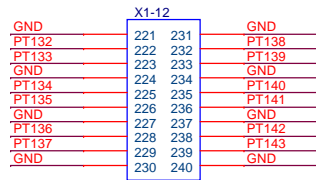
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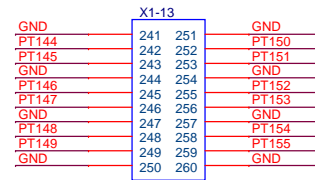
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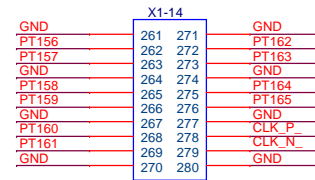
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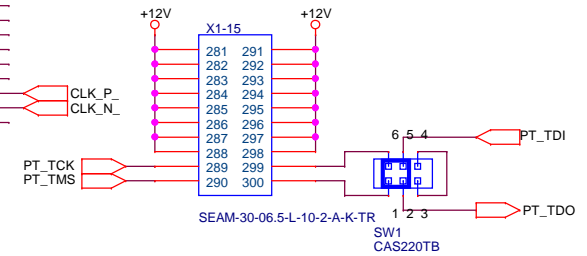
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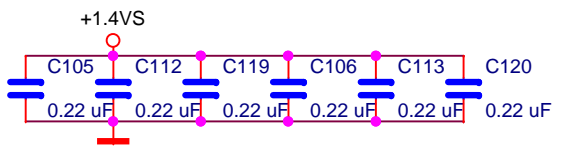
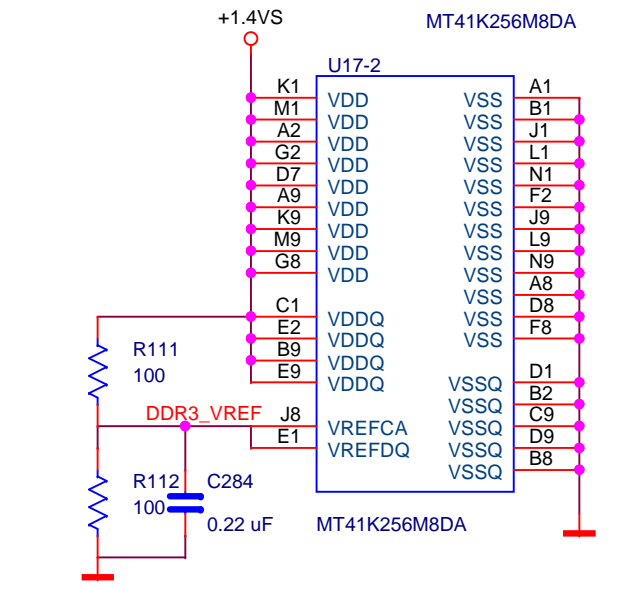
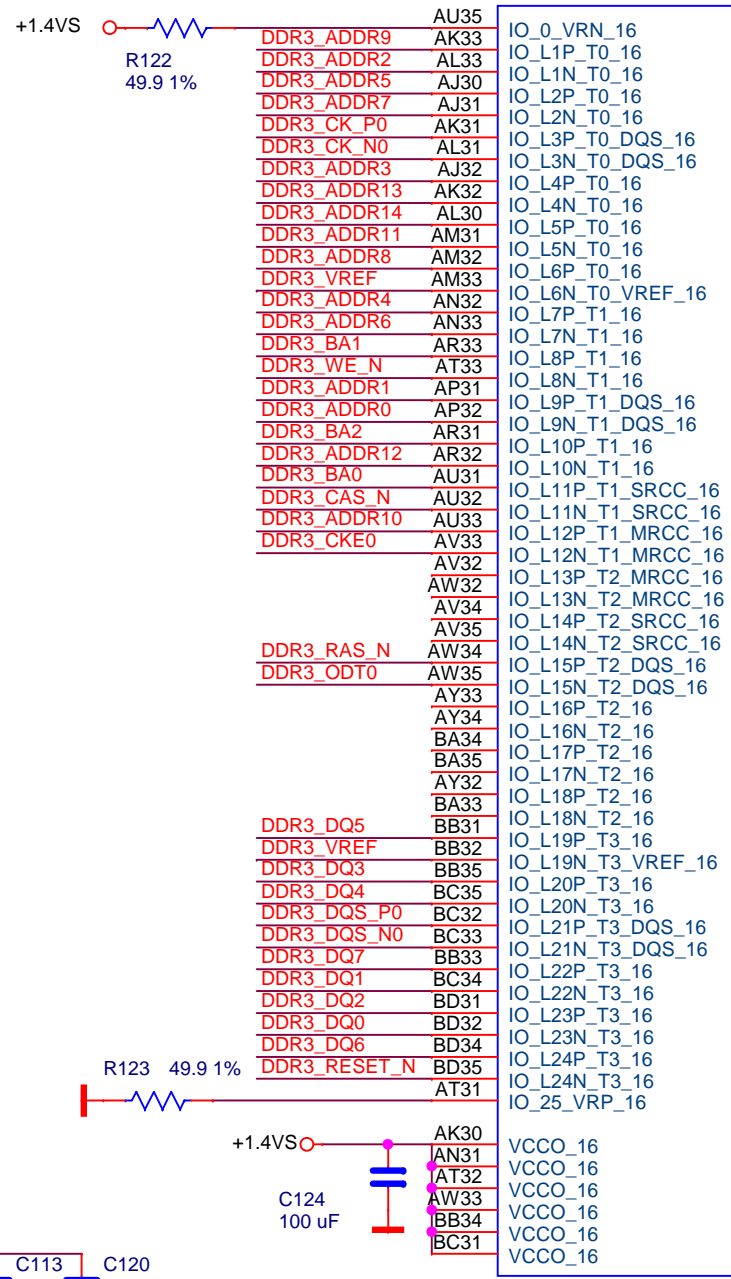
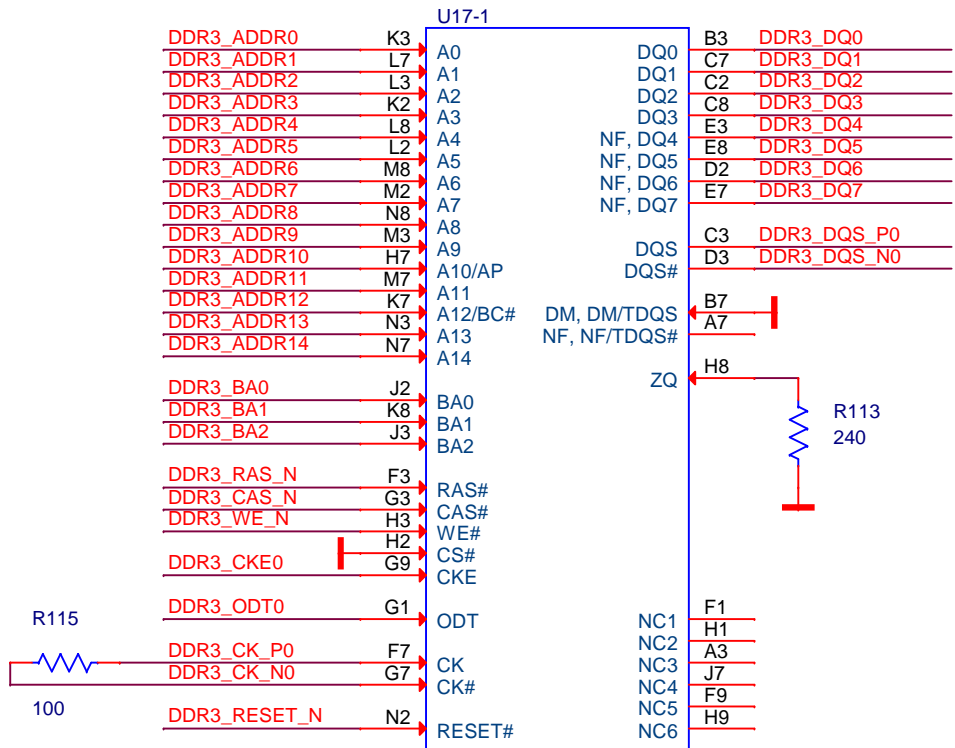


Mezzanine standoffs



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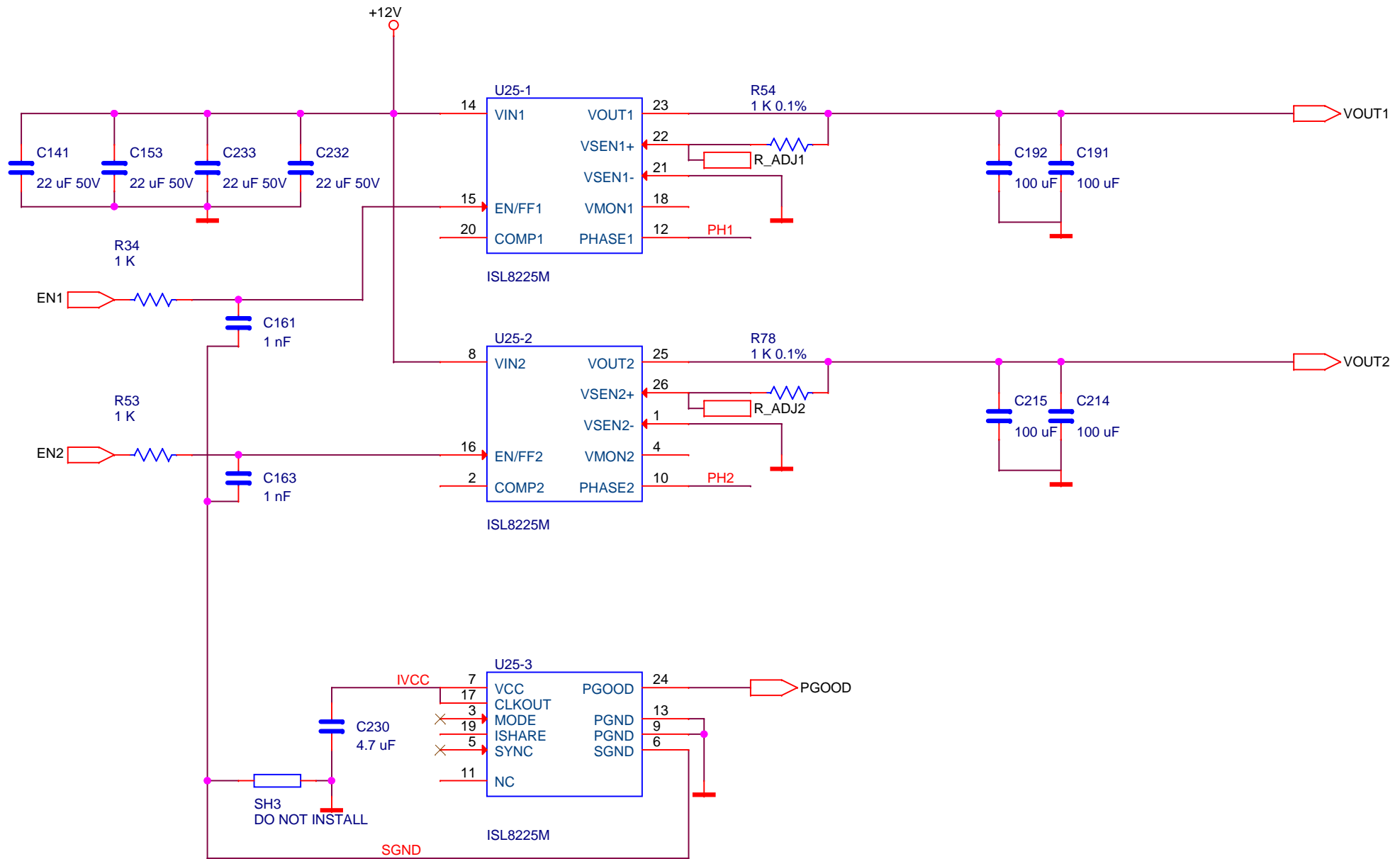
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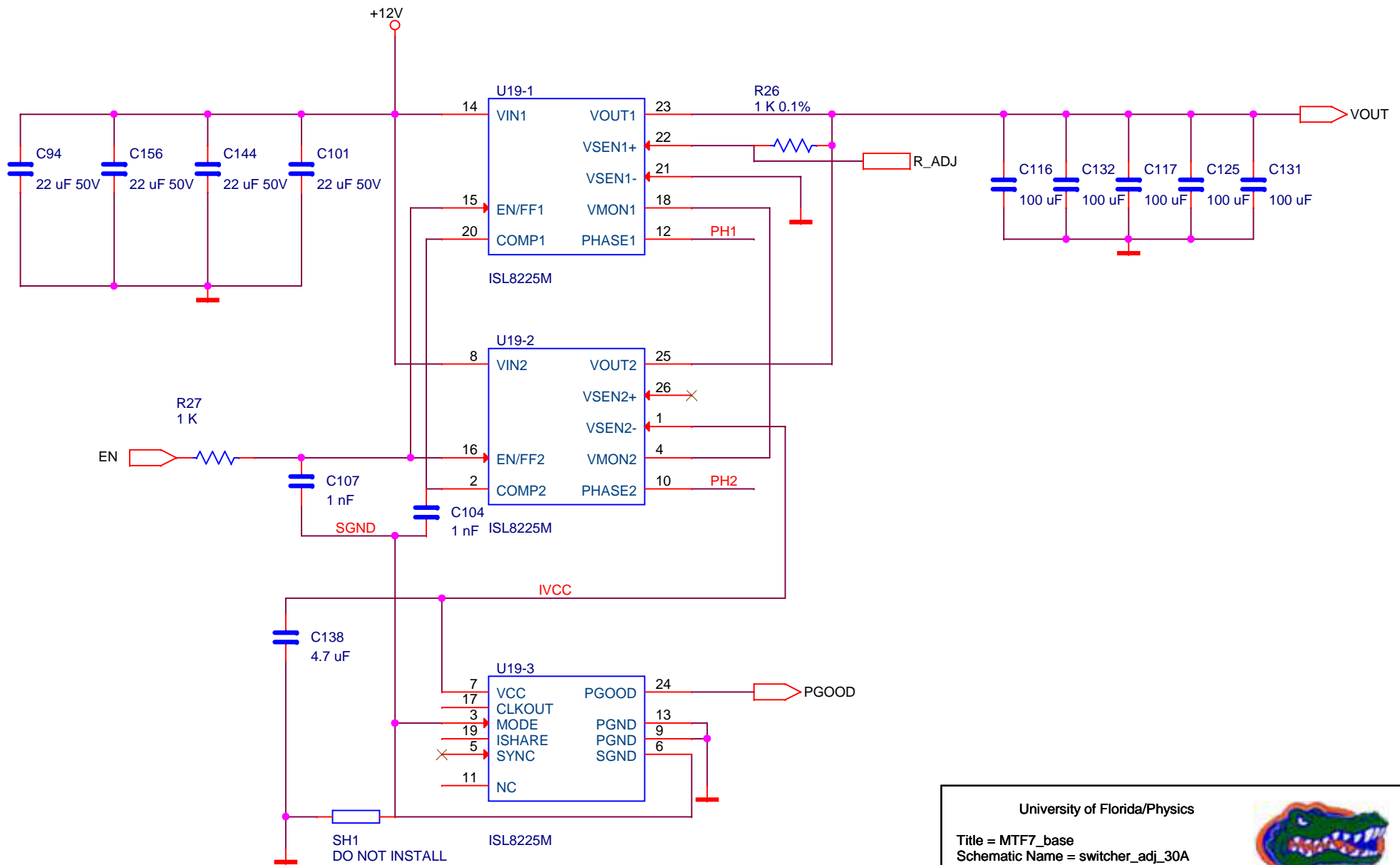
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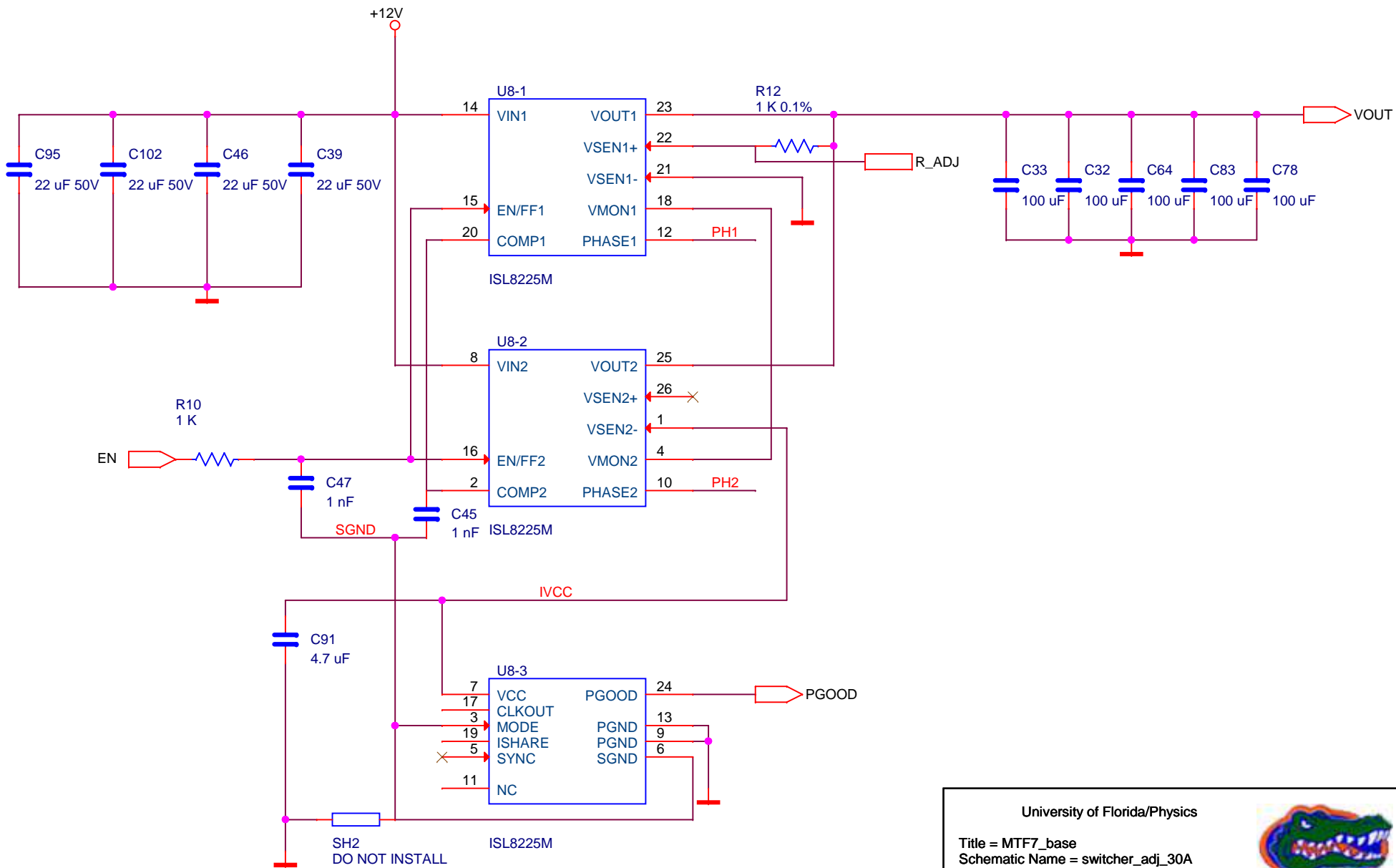


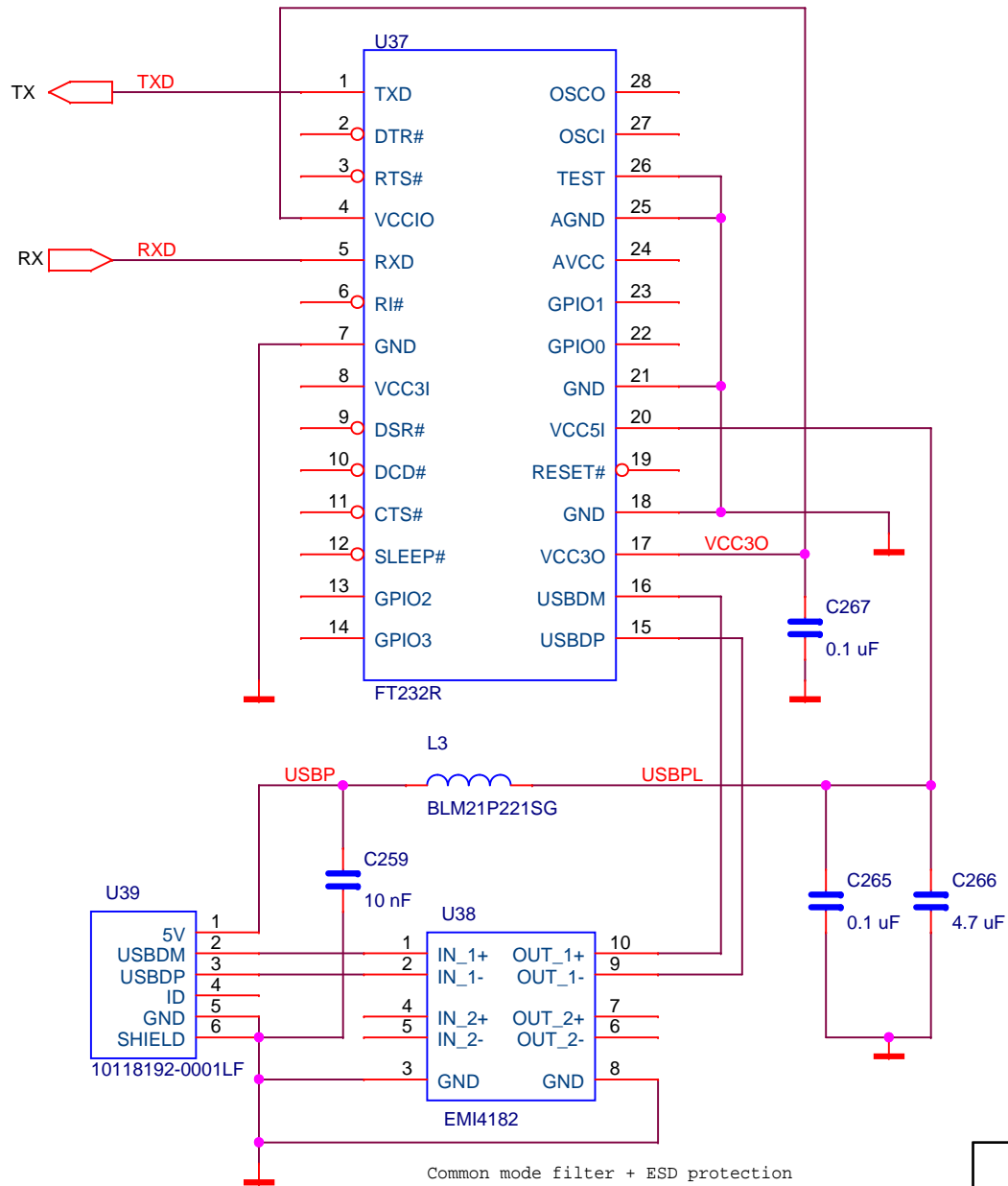
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Common mode filter + ESD protection

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