Mezzanine SERDES Board Specification

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The SERDES (Serializer/Deserializer) is a mezzanine card that comprises the Texas Instruments TLK Multigigabit Transceiver device [1] and a Small Form Factor Pluggable (SFP) optical module [2]. The pictures of the board are shown in Fig.1. The list of suitable pin compatible TLK transceivers is given in Table 1.

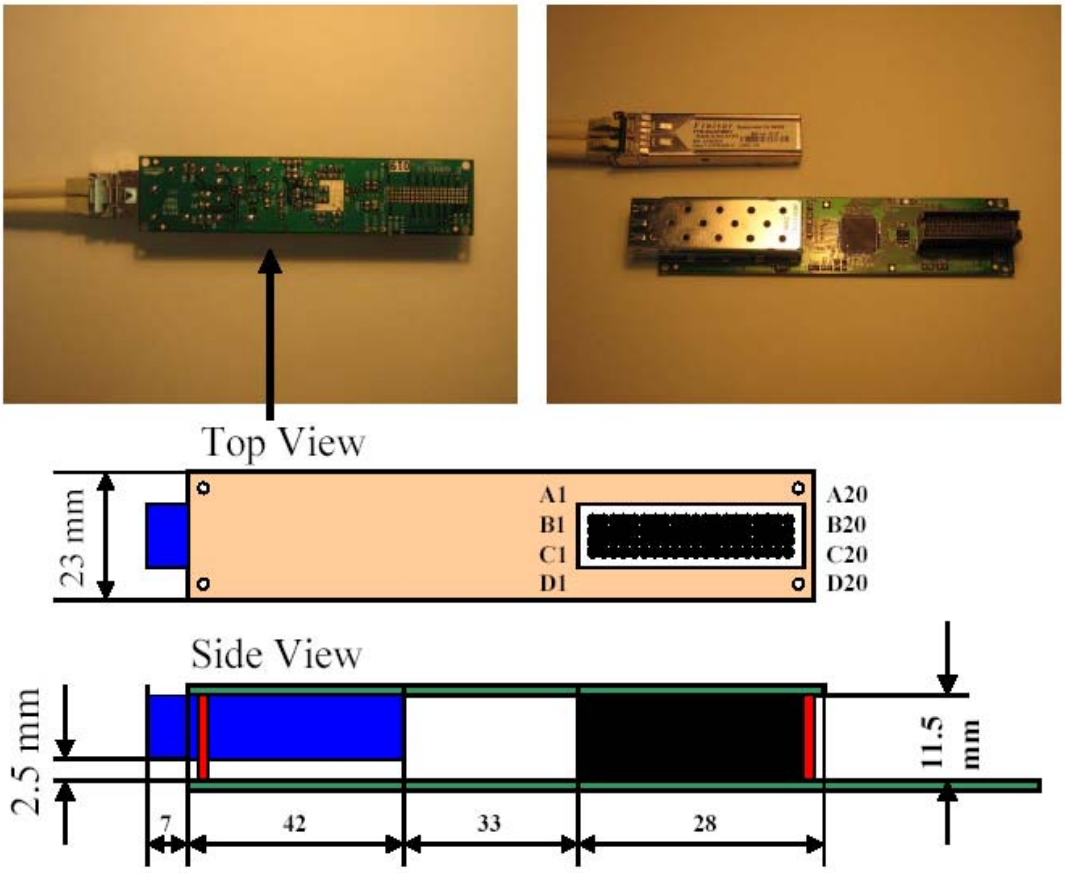

Figure 1: SERDES views (top and bottom) and PCB dimensions

The interface to a host board consists of 16-bit transmitter and 16-bit receiver paths and several control and status signals for the TLK and SFP transceivers. The main reference clock for the TLK transceiver (INCLK) is provided from the host board. For reliable transmission the jitter requirements (see datasheets) must be observed. The Samtec MOLC-120-31-S-Q 80-pin connector is used on SERDES card and the Samtec FOLC-120-01-S-Q socket should be used on a host board. The list of signals is shown in Table 2. The signal names represent the interface to TLK1501/2501/3101 devices. For other TLK transceivers (Table 1) some of the control and status signals have to be reassigned. For more details see the TLK datasheets.

Table 1

Part Number	Parallel Bus, bit	Serial Interface	Bit Rate, Gbps	Reference Clock Frequency, MHz	Encoding Method	Embedded PRBS generator
TLK1501	16	CML*	0.6-1.5	30-75	8B/10B	2^7-1
TLK2501	16	CML*	1.5-2.5	75-125	8B/10B	2^7-1
TLK3101	16	VML*	2.5-3.125	125-156.25	8B/10B	2^7-1
TLK1521	18	VML*	0.5-1.3	25-65	Start/Stop	None
TLK2521	18	VML*	1.0-2.5	50-125	Start/Stop	None
TLK2701	16	CML*	1.6-2.7	80-135	8B/10B	2^7-1
TLK2711	16	VML*	1.6-2.7	80-135	8B/10B	2^7-1

* CML – Current Mode Logic, VML – Voltage Mode Logic, for more details see TI Application Report SLLA120 available at http://focus.ti.com/lit/an/slla120/slla120.pdf

Table 2

Pin	Signal	Dir	Pin	Signal	Dir	Pin	Signal	Dir	Pin	Signal	Dir
A1	INCLK	I	B1	GND		C1	GND		D1	OUTCLK	O
A2	GND		B2	*RATE*	I	C2	*LOS*	O	D2	GND	
A3	TXD0	I	B3	LOOPEN	I	C3	PRBSEN	I	D3	RXD0	O
A4	TXD1	I	B4	+3.3V		C4	RXD1	O	D4	+3.3V	
A5	+3.3V		B5	TXD2	I	C5	+3.3V		D5	RXD2	O
A6	TXD3	I	B6	+3.3V		C6	RXD3	O	D6	+3.3V	
A7	+3.3V		B7	TXD4	I	C7	+3.3V		D7	RXD4	O
A8	TXD5	I	B8	GND		C8	RXD5	O	D8	GND	
A9	GND		B9	TXD6	I	C9	GND		D9	RXD6	O
A10	TXD7	I	B10	GND		C10	RXD7	O	D10	GND	
A11	GND		B11	TXD8	I	C11	GND		D11	RXD8	O
A12	TXD9	I	B12	+2.5V		C12	RXD9	O	D12	*MODDEF1*	I
A13	+2.5V		B13	TXD10	I	C13	+2.5V		D13	RXD10	O
A14	TXD11	I	B14	+2.5V		C14	RXD11	O	D14	+2.5V	
A15	+2.5V		B15	TXD12	I	C15	+2.5V		D15	RXD12	O
A16	TXD13	I	B16	*TDIS*	I	C16	RXD13	O	D16	*TFAULT*	O
A17	GND		B17	TXD14	I	C17	GND		D17	RXD14	O
A18	TXD15	I	B18	GND		C18	RXD15	O	D18	PWFAULT	O
A19	TXEN	I	B19	*MODDEF2*	I	C19	TXER	I	D19	RXER	O
A20	ENABLE	I	B20	*MODDEF0*	I	C20	LCKREFN	I	D20	RXDV	O

Comments

1. Direction (Dir): I (Input) and O (Output) in respect to the SERDES mezzanine card
2. Signals shown in blue are for the TLK device. Signals shown in green *(italic)* are for the SFP module. Signal PWRFAULT is a status output of the National Semiconductor LP3982 voltage regulator.

The TLK devices require +2.5V and the SFP module require +3.3V power. While +3.3V power must be provided from the host board, the +2.5V power can be provided from the host board (jumper JP3 2-3 installed) or obtained from the voltage regulator (up to 300 mA), when jumper JP3 1-2 is installed. The PWRFAULT status output of the LP3982 voltage regulator is available for monitoring on a host board.

Five signals MODDEF[0-2], LOS and TFAULT related to SFP module have pull-up resistors on the SERDES card. The signals TDIS can be connected to GND with the 0805 type surface mounted jumper JP1 to permanently enable the SFP transmitter. The RATE signal of the SFP can be connected to GND with the 0805 type surface mounted jumper JP2 as well (for reduced bandwidth).

The size of the board is 104 mm (length) x 23 mm (width) x 13.7 mm (height). Normally, the 80-pin Samtec connector is mounted on the same side of the PCB as the TLK device, voltage regulator, and the SFP cage (Fig.1). When the mezzanine is installed on a host board, these parts are facing the top of the host board (Fig.1). The clearance between the SERDES mezzanine and a host board is 11.5 mm which is sufficient for air cooling of both TLK transceiver and voltage regulator. However, for some special applications the Samtec connector can be installed on the bottom side of the mezzanine as well. The layout of the host board should reflect this option. Up to 3 SERDES mezzanines can be installed on a PCI card, up to 8 on a 6U VME/cPCI card, and up to 14 near the front panel of the 9U VME card (Fig.2).

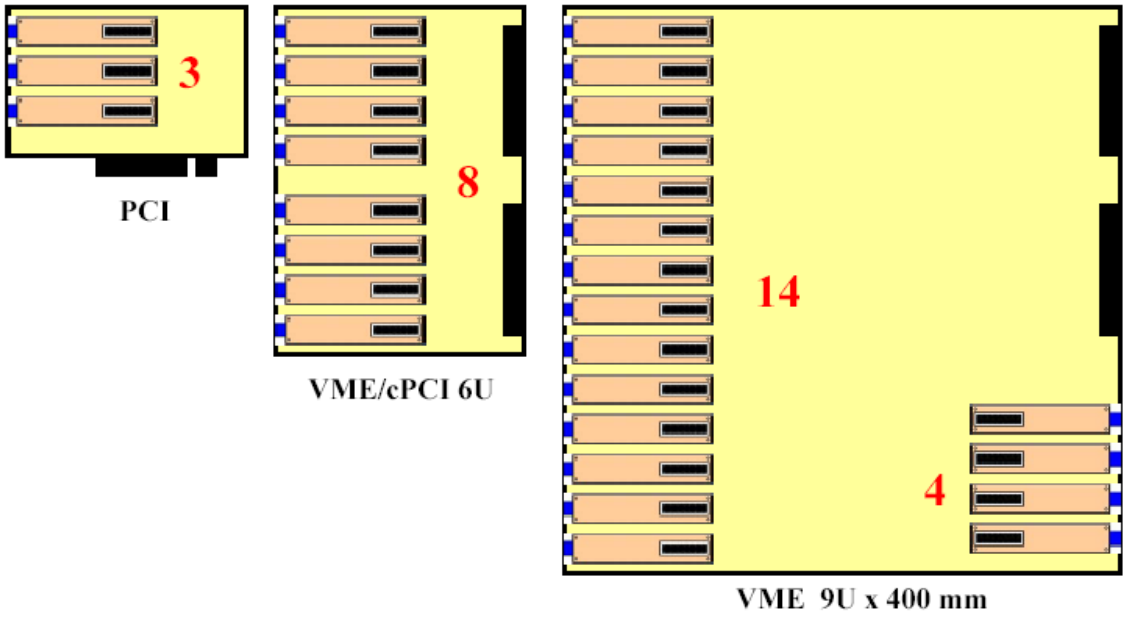

Figure 2: Possible applications of the SERDES mezzanine card

The total power consumption depends on the TLK device and the SFP module (consult datasheets), but typically doesn't exceed 230 mA @ 2.5V (for the TLK3101 at highest operating frequency) and 200 mA @ 3.3V (optical SFP transceiver).

The main advantage of the SERDES card is that it is a compact and inexpensive mezzanine for data serialization, transmission and deserialization that can be used on both ends of the transmission link in wide frequency range. Such a pre-engineered solution allows to save space and simplify the design and layout of the host board and avoid using of +2.5V power when it's not needed for other components on the host board. The estimated cost of the mezzanine (including components and services, but

excluding the SFP module) is below $100. Sample boards with the TLK1501/2501/3101 devices are available immediately.

References

[1] Texas Instruments General Purpose Gigabit Transceivers. http://focus.ti.com/paramsearch/docs/parametricsearch.tsp?family=analog&familyId=553&uiTemplateId=NODE_STRY_PGE_T
[2] SFP Specification. ftp://ftp.seagate.com/sff/INF-8074.PDF