The synchronous sorter “2 out of 12” receives 12 8-bit patterns every clock cycle, selects two best (largest) patterns and transmits them to the output. The project comprises 6 design files, all written in VHDL. At a first step, all comparisons (12x11/2=66) (comps66.vhd) between patterns are performed. At a second step, the results of comparisons are used to define the 12-bit binary addresses of the 1st and 2nd best patterns (see block diagram on Fig.1). Finally, at a third step, the outputs of the select1.vhd and select2.vhd are used to merge 12 patterns into 2 best. All inputs and outputs are latches into flip-flops.

If several patterns appear to have the same value, then a pattern with higher number will be chosen as the best one. For example, if Pattern_7 and Pattern_11 have the same value, then Pattern_11 will be selected as a first best and Pattern_7 as a second best. Although the process of selection is sequential (select2 requires outputs from select1), each select[i] design comprises simple combinatorial logic and the overall latency is low.

The design was synthesized and implemented with Xilinx ISE 5.1.02 software. The performance was 67.01 MHz for XC2V2000-5BG728 FPGA and 77.13 MHz for smaller XC2V250-5FG256 FPGA.