The synchronous sorter “4 out of 24” receives 24 6-bit patterns every clock cycle, selects four best (largest) patterns and transmits them to the output. The project comprises 10 design files, all written in VHDL. At a first step, all comparisons (comps276.vhd) between patterns are performed. At a second step, the results of comparisons are used to define the 24-bit binary addresses of the 1st, 2nd, 3rd and 4th best patterns (see block diagram on Fig.1). Finally, at a third step, the outputs of the select1.vhd, select2.vhd, select3.vhd and select4.vhd are used to merge 24 patterns into 4 best. All inputs and outputs are latches into flip-flops. The design was optimized to run at clk1=40Mhz, so pipeline registers were added between select2 and select3 stages (Fig.1).

If several patterns appear to have the same value, then a pattern with higher number will be chosen as the best one. For example, if Pattern_23 and Pattern_11 have the same value, then Pattern_23 will be selected as a first best and Pattern_11 as a second best. Since the top design file sorter24.vhd is relatively small, it can be easily modified for patterns with different width and optimized for another clock frequency (with adding or removing pipeline flip-flops). Although the process of selection is sequential (select2 requires outputs from select1, select3 requires outputs from select1 and select2 and so on), each select[1..4] design comprises simple combinatorial logic and the overall latency is low.

Fig 1. Block Diagram of the sorter24 project